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Detection of the location of the hazard during and after the design of combinational circuits

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Abstract. Delay fault and glitch fault cause hazards that are structure hazard and function hazard. During design process we can use many methods to identify and remove structural hazard [1-2], [3]. However, with function hazards, determination and remove much more difficult. In this paper we introduce a new solution to determine the structure hazard by the Truth table - Matrix mathematics Method and method for determining function hazard over how to determine crosstalk fault [4-7].

Keywords: Structure hazard, function hazard, truth table, multiplication matrix, hazard – algebra, crosstalk fault, glitch.

1. Introduction

Detecting, locating and removing hazards in a digital circuits is the compelling work of a designer. Karnaugh map [8] was used very often to design digital circuits that are combinational and sequence; synchronous and asynchronous with hazard – free.

John Knight [1], [3], Thuong N.Q [2] applied hazard – algebra method for the design of digital circuits. If a circuit has a hazard, then function of the circuit will be reduced to one of these forms $x\bar{x}$, $x+\bar{x}$, $x\bar{x}+x$ and $(x+\bar{x})x$. Hazard – algebra method can detect and mask hazard in both combinational and sequence circuits.

To investigate hazard in combinational circuits with EX – OR gates, E.C. Tan and M.H. Ho [9] built matrix method that generate a set of variables of all nodes in each gate level of a circuit progressively until it reaches the output of circuit. However, this method has notyet show exact location of hazards and when dynamic hazard is dependent on static logic 0 – hazard or dependent on static logic 1 – hazard. [4-7], [10,11] shows the test methods for crosstalk fault induced glitch fault. Through crosstalk fault, we have function Hazards can be determined, that appears only after the circuit was put into use.

In this paper a new solution is proposed to investigate structure hazards in combinational circuits that is based on combination of truth table, matrix mathematics and hazard - algebra to detect structure

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hazards. This paper also points out the method of determining the function hazards via the determination of crosstalk fault. The structure of this paper is as follows. Section 2 gives background on hazard algebra, the difference between Boolean algebra and Hazard algebra; relations between matrix mathematics and truth table and circuit equation of function; the test methods to determine the crosstalk fault, which is to determine function hazard in the digital circuit. Section 3 gives the formal problem statement to be solved, and an intuitive overview of the new method as the rules to detect structure hazards of sophisticated forms (including SOP and POS). Section 4 gives the mode of determining the function hazard in the circuit was put into use.

2. Background

The potential for a glitch in a combinational circuit is called a hazard. Hazards fall into two classes: function hazards and structural hazards. Structure hazard could be detected and removed even during the design process but function hazard that can detect only the circuit after having taken into use and the removal of function hazard is more difficult than of structural hazard. This section focuses on the problem to of hazards, hazard algebra, matrix mathematics and crosstalk fault.

2.1. Truth table – Matrix Mathematics Method for the detection and location of structure hazards in digital circuits

Truth table – matrix mathematics method was built to the detection and location hazards in combinational circuits that is expressed in either sum-of- products (SOP) form or product-of-sums (POS) form or both. The main idea of this work is to "dip" *the variables of function* on *their truth table* by multiplying these matrices conform to the rules of multiplication matrix (mathematics). The result of the multiplication is compared with definitions of hazards in hazard algebra [1], [2], [3]. That is $\xi = \tau^H.\tau^L = \xi(0)$ as *static 0 - hazard,* $\xi = \tau^H + \tau^L = \xi(1)$ as *static 1 - hazard and* $\xi = \tau^H.\tau^L + \tau^H = \xi_0(0)$, $\xi = (\tau^H + \tau^L).\tau^H = \xi_0(1)$ as dynamic hazard dependent on static 0- hazard and dynamic hazard dependent on static 1- hazard, respectively.

The principle of this method as follows: firstly we find the variables x that can cause hazard, and then fix value 0 or 1 in variables $x_i \neq x$. To realize this problem we can "dip" the variables, the sum factors or the product terms of circuit equation on the truth table n variables based on multiplying *equation - matrix* with *truth table - matrix* that conform to the rules of multiplication matrix (mathematics).

The *equation - matrix* is a matrix express circuit equation. If circuit equation in form SOP, then circuit equation will holds sum factors and if circuit equation in form POS, then circuit equation will holds product terms. Number of sum factors or product terms in these circuit equations shows number columns of matrix, that is, matrix with dimensions 1xn that is matrix with 1 row and n columns.

The *Matrix truth* table is a matrix express truth table of circuit function. In this method the truth table is reputed to be a matrix n x 2^{n-1}, it means matrix with n columns and 2^{n-1} rows.

To make number of columns in circuit equation - matrix equal to number of rows in truth table – matrix we can change this matrix into *transpose matrix*, that is, let A be an n x 2^{n-1} matrix defined by the number a_{ij}, then the transpose of A as A^T, denoted A^T is the 2^{n-1} x n matrix defined by the number b_{ij} where $b_{ji} = a_i$

The algorithm to detect structure hazards in combinational circuit of this method is given as follows:

Step 1: Consider the circuit equation.

If the circuit equation is complicated, then apply De Morgan Law to get the simplest circuit equation that are circuit equations in forms either SOP or POS or both.

Step 2: Consider the variables.

- Firstly, find the variables that can cause hazards. They are those variables having both x and $\bar{x}$ form, in this case x:= τ^H and x':= τ^L are independent.

Fix $x_i \neq x(\tau^H,\tau^L)$ values (0,1) by "dip" circuit equation n variables on the truth table of circuit function respectively that realized by multiplying two matrices that are *circuit equation - matrix* and *truth table – matrix*.

Step 3: Consider the result of multiplication

After the variables $x_i \neq x(\tau^H,\tau^L)$ are fixed value 0 or 1 by "dip" circuit equation n variables on the truth table so we get the result of multiplication that either the sum factors $\tau^H.\ \tau^L = \xi(0)$, the circuit contains static – 0 hazard, or the product terms $\tau^H + \tau^L = \xi(1)$, that is the circuit contains static – 1 hazard, or dynamic hazard dependent on static logic 0 – hazard $\xi = \tau^H.\ \tau^L + \tau^H = \xi_0(0)$ and dynamic hazard dependent on static logic 1 – hazard $\xi = (\tau^H + \tau^L).\tau^H = \xi_0(1)$, or not at all, that is the free hazard circuit.

Step 4: Investigate to remaining variables

To find the remaining variables x_i that can cause hazards. Go to Step 2, Step 3 until last variable x_i is considered.

2.2 To detect crosstalk fault induced function hazards

After the digital circuit is designed and built, it is always desirable to know whether the circuit is constructed without any faults. Is it is properly constructed and in use, it may be disable by almost any internal failure. The process of applying test and determining whether a digital circuit is fault free or not is known as fault detection. If we known relationship exists between the various possible faults and deviations of output patterns, is termed as fault location [12] as *function hazard*. The increased design density in deep – submicron designs leads to more significant interference between the signals because of capacitive coupling or crosstalk. Crosstalk can induce both Boolean errors and delay faults. Crosstalk – induced pulses are likely to cause errors on hazard – sensitive lines such as inputs to dynamic gates, clock, set/reset and data inputs to flip – flops. Crosstalk pulses might result in logic errors or degraded voltage levels, which increase propagation delays [6].

Studies show that increased coupling effects between signals can cause signal delay to increase (slow down) or decrease (speed up) significantly. Both conditions can cause errors. Signal slow down can cause *delay faults* if a transition is propagated along paths with small slacks. Signal speed - up can cause *race (glitch) conditions* if a transitions are propagated along short paths [6]. Crosstalk glitch occurs when there is a switch for the signal at one line and the signal at the other line is driven steady, in which case a glitch is formed at the output of the steady line. The condition for crosstalk delay is that the signal at both line switches to the opposite direction. The result is an increase in transition time [5]. For two line in a circuit, if the signal transition of 0 to 1 or 1 to 0 on a line produces coupling effects on another line, then the signal line is called an aggressor line, and the other line is called a victim line. For instance, if the victim line and aggressor line are driven respectively by a static 0 and a

fast – rising (0 to 1) transition, then the crosstalk positive glitch is generated in the victim's output signal. If the height of crosstalk glitch happens to be larger than the upper – threshold value of logic – low voltage for the give technology, it will produce logic failures (*functionality problem*) [6]. We consider the function hazard in digital circuit, was put into use, as detect the crosstalk faults. Here we define crosstalk fault on digital circuits by using Binary Decision Diagram (BDD) of [6].

So if we want to detect all forms of hazard in the circuit so, then we need to determine structure hazards within the design process and function hazard by determining the crosstalk fault.

3. Detection structure hazard in combinational circuits

From definitions of hazard and the algorithm to detect hazard of this method in section 2 now we can find hazards in circuits for sum - of - products implementation, or for product - of - sums implementation, or complicated circuit that is not only in form POS or SOP but also hold all POS and SOP. Let us consider an EX – OR gate [9] (Fig. 5) as complex circuit

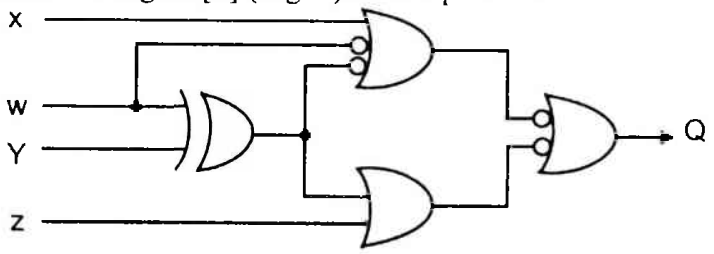

Fig. 1. Circuit with EX – OR gate.

Step 1: From this circuit we have circuit equation:

$$Q = \overline{\overline{\overline{X}Y + X\overline{Y}} + \overline{X} + W + \overline{\overline{X}Y + X\overline{Y}} + Z}$$

Use the Boolean relations to change circuit equation, we get:

$$Q = (\overline{X}Y + X\overline{Y})X\overline{W} + (X + \overline{Y})(\overline{X} + Y)\overline{Z}$$

Step 2: The Circuit equation has two variables $X(\tau^L,\tau^H)$ and Y (τ^L,τ^H) can cause hazard. Firstly, consider for X:

$$X := (\tau^H,\tau^L)$$
$$(Y,Z,W) := (0,1)$$

The equation Q has two *sum factors* that are $(\overline{X}Y + X\overline{Y})X\overline{W}$ and $(X + \overline{Y})(\overline{X} + Y)\overline{Z}$ (in form SOP), but in one sum factor hold *product terms* (POS). Example: sum factor $(\overline{X}Y + X\overline{Y})X\overline{W}$ hold two product terms $(\overline{X}Y + X\overline{Y})$ and $X\overline{W}$ (POS and SOP). So we can create from circuit equation Q to one matrix M with two product terms $(\overline{X}Y + X\overline{Y})$, $X\overline{W}$ and one sum factor $(X + \overline{Y})(\overline{X} + Y)\overline{Z}$

$$M.A^T = \left[(\overline{X}Y + X\overline{Y}) \quad (X\overline{W}) \quad (X + \overline{Y})(\overline{X} + Y)\overline{Z}\right] . \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}$$

Also result of multiplication in a column is defined by addition (AoC) for sum factors and multiply (MoC) for product terms. Example, result of multiplication in first column of below $M.A^T$ is $(\tau^H).(\tau^H)+\tau^L = (\tau^H)+\tau^L$. So we get:

$$M.A^T = \begin{bmatrix} (\tau^H) & (\tau^L) & (\tau^H) & (\tau^L) & (\tau^H) & (\tau^L) & (\tau^H) & (\tau^L) \\ (\tau^H) & (\tau^H) & (0) & (0) & (\tau^H) & (\tau^H) & (0) & (0) \\ \tau^L & \tau^L & \tau^L & \tau^L & 0 & 0 & 0 & 0 \end{bmatrix} \begin{matrix} Y \\ Z \\ W \end{matrix}$$

$$= \begin{bmatrix} (\tau^H)+\tau^L & (\tau^H).(\tau^L)+\tau^L & \tau^L & \tau^L & (\tau^H) & (\tau^L).(\tau^H) & 0 & 0 \end{bmatrix}$$

$$\Downarrow \qquad \Downarrow \qquad \Downarrow$$

$$\xi(1) \text{ in } \begin{cases} Y=0 \\ Z=0 \\ W=0 \end{cases} \qquad \xi_\theta(1) \text{ in } \begin{cases} Y=1 \\ Z=0 \\ W=0 \end{cases} \qquad \xi(0) \text{ in } \begin{cases} Y=1 \\ Z=0 \\ W=1 \end{cases}$$

Compare with Definition 1 and 2 we find out one static – 0 hazard $\xi(0)$ in Y = W = 1, Z = 0, one static – 1 hazard $\xi(1)$ in Y = Z = W = 0 and one dynamic hazard dependent static – 1 hazard $\xi_\theta(1)$ in Y = 1, Z = W = 0.

Step 4: Go to Step 2, Step 3 to consider variable Y:

$$Y := (\tau^H, \tau^L)$$
$$(X,Z,W) := (0,1)$$

we get the result of multiplication:

$$M.A^T = [M] . \begin{bmatrix} 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}$$

$$\Downarrow \qquad \Downarrow \quad \Downarrow$$

$$= \begin{bmatrix} (\tau^H) & (\tau^H) & (\tau^H) & (\tau^H) & (\tau^L) & (\tau^L) & (\tau^L) & (\tau^L) \\ (\tau^H) & (\tau^H) & (0) & (0) & (\tau^H) & (\tau^H) & (0) & (0) \\ \tau^L & 0 & \tau^L & 0 & \tau^L & 0 & \tau^L & 0 \end{bmatrix} \begin{matrix} X \\ Z \\ W \end{matrix}$$

$$\begin{bmatrix} (\tau^H)+\tau^L & (\tau^H) & \tau^L & 0 & (\tau^H)(\tau^L)+\tau^L & (\tau^H)(\tau^L) & 0 & 0 \end{bmatrix}$$

$$\Downarrow \qquad \Downarrow \qquad \Downarrow$$

$$\xi(1) \text{ in } \begin{cases} X=0 \\ Z=0 \\ W=0 \end{cases} \qquad \xi_\theta(0) \text{ in } \begin{cases} X=0 \\ Z=0 \\ W=1 \end{cases} \qquad \xi(0) \text{ in } \begin{cases} X=1 \\ Z=0 \\ W=1 \end{cases}$$

we have identified hazards $\xi(1) \in \left(X=Z=W=0\right)$, $\xi(0) \in \left(X=W=1, Z=0\right)$ and $\xi_{\theta}(0) \in (x=1,\ z=w=0)$

Thus, the circuit function Q has not only dynamic hazard [9], but also static – 1 hazard and static - 0 hazard.

4. Detection Crosstalk induced function hazard

To determine the glitch in the circuit than we need to identify the crosstalk fault. In principle to determine the stuck at fault or crosstalk fault is to create the test vector. If there is a fault in a circuit, then the test vectors of the fault are the input assignments that cause the faulty circuit and normal circuit (fault – free circuit) to produce different output values. The test vector distinguish between the good machine and the faulted machine. So the test vector is built, which is the XOR operation of the fault – free circuit and faulty circuit. Figures 2 [10] tells us more about this in Functional Equivalence and Functional Dominance (Functional Collapsing): For an input vector, V, to be a test for a fault, we have:

$$F_0(V) \oplus F_1(V) = 1$$

where F_0 is the fault – free function and F_1 is the faulty function, respectively. Consider a second fault that produces a fault function F_2. According to the definition of fault equivalent faults have exactly the same tests. Therefore, for two faults to be equivalent, we have

$$[F_0(V) \oplus F_1(V)] \oplus F_2(V)] = 0 \Rightarrow F_1(V)] \oplus F_2(V) = 0$$

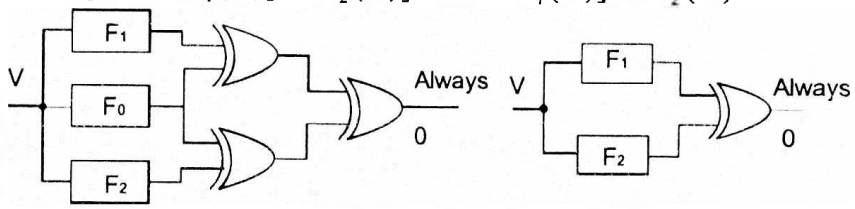

Fig. 2. Viewing fault Equivalence.

In [6] test vector is called test BDD (Test Binary Decision Diagram), normal circuit are known as normal BDD and faulty circuit is faulty BDD, so we have test BDD:

$$\text{Test BDD} = \text{normal BDD} \cdot \overline{\text{faulty BDD}} + \overline{\text{normal BDD}} \cdot \text{faulty BDD} = 1$$

In the test BDD, each input assignment with attribute value 1 is a test vector of the fault.

The crosstalk fault is one of the interference effects being caused by parasitic capacitance and inductance coupling. For two line in circuit, if the signal transit of 0 to 1 or 1 to 0 one line produces coupling effects on another line, then the line is called an aggressor line, the other is called a victim line. Figure 3 shows the relationship between aggressor line and victim line [11].

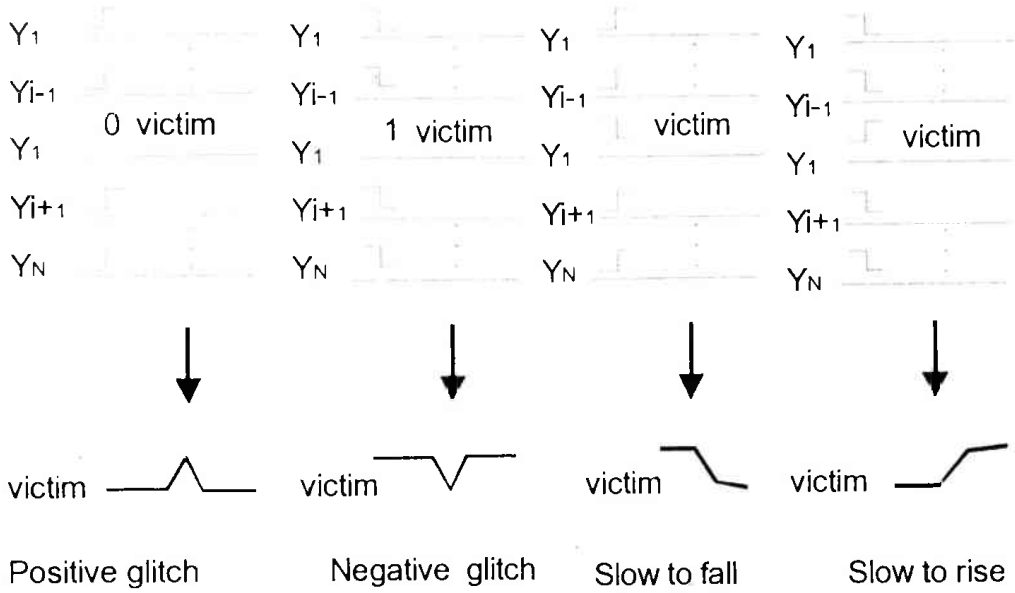

Fig. 3. Maximal aggressor fault model.

The Positive glitch and Negative glitch in Fig. 3 are function hazards. These Hazards can not be removed during the design process, because they appear only after having taken into use.

Here, for circuit C17 [6] shown in Fig. 4, we give an example for test generation when there is a crosstalk fault between signal lines e_3 and e_4. The task of test generation is to search for the inputs vectors of circuit C 17 in order to detect the crosstalk fault. For example, a test vector of the crosstalk fault is made up of circuit input vectors $V_1 = (x_1, x_2, x_3, x_4, x_5) = (0, 0, 0, 0, 0)$ and $V_2 = (x_1, x_2, x_3, x_4, x_5) = (0, 0, 0, 0, 1)$. Apply V_1 and V_2 to the circuit sequentially. If the circuit outputs are $y_1 = 0$ and $y_2 = 0$ for V_1, $y_1 = 0$ and $y_2 = 1$ for V_2,, then there is not crosstalk. If the circuit outputs are $y_1 = 0$ and $y_2 = 0$ for V_1, $y_1 = 1$ and $y_2 = 1$ for V_2,, then there is crosstalk. Therefore, this test vector can detect the crosstalk fault between e_3 and e_4. Here, assume that $e_4$is a aggressor line and e_3 is a victim line, and that a down transition (1 to 0) in signal line e_4 produces a glitch (1 to 0) in signal line e3, that is, there is a function hazard.

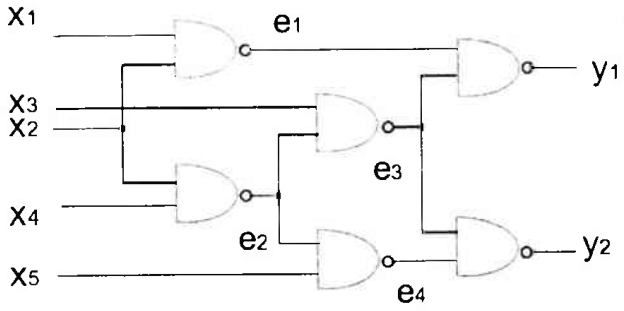

Fig. 4. C17 Circuit.

5. Conclusion

The detection, locate and remove the Hazards of the digital circuits is very critical for circuit designers. Structure hazard are detected and removed even during the design process and there were some methods to solve this. Truth table – Matrix Mathematics Method presented here is a new solution to investigate structure hazard. This method not only detected all kinds hazards in combinational circuits but also point out location of hazards with high accuracy. The Truth table – Matrix Mathematics can detect hazard in all circuit functions that can expressed by truth table. The removing structure hazard errors no difficulty if we use Karnaugh map [8] or hazard algebra [1-3] to supply redundant terms corresponding each kind of hazard. These function hazard can not be removed during the design process, because they appear only after having taken into use. Duration of function hazard can permanent, temporary or intermittent, thus removing it is not easy. We can determine function hazard, for example through the identification of crosstalk fault as described above.

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