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Verification of hazard, race and deadlock in GALS-circuit

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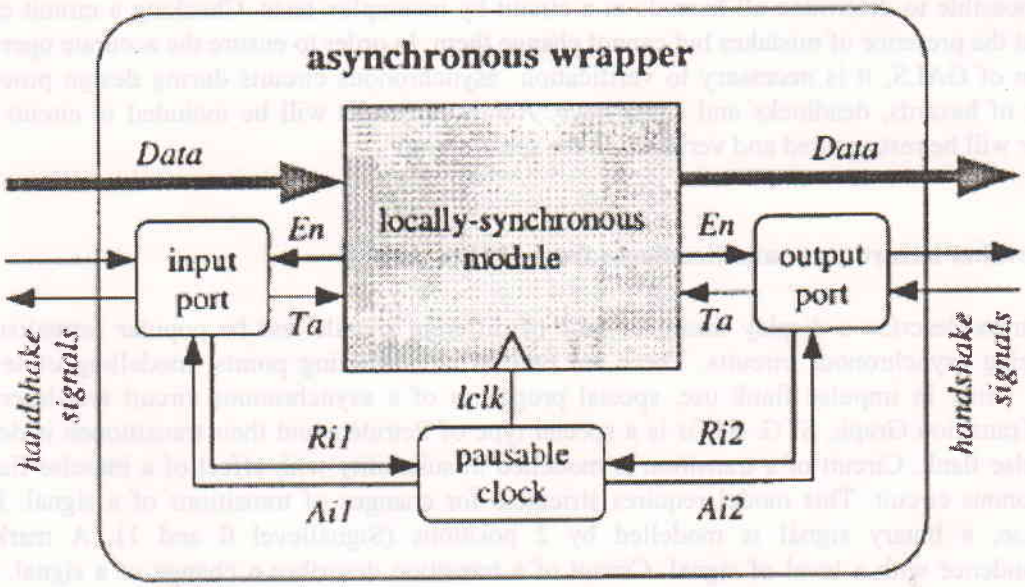
Abstract. It is not easy to point out Hazards and Deadlock in a circuit with a complex structure. Determination methods for Hazard, Race, Deadlock in [1-3] cannot be applied to this case. With complex circuit structure, specific solution must be offered for each circuit type such as solution of synchonization for asynchronous circuits [4]. GALS circuit is a complex circuit system; thus, the above-mentioned solution is also applied to this circuit.

1. Introduction

GALS (Global Asynchronous - Local Synchronous) is a combined system. In order to create GALS, the system is divided into many moduls which are independent in respect of time (local - synchro), these moduls are included in one wrapper (global - asynchrone). Image of a GALS - block is shown in Figure 1 [5].



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And asynchronous wrappers connect together, as show on Figure 2 [5].

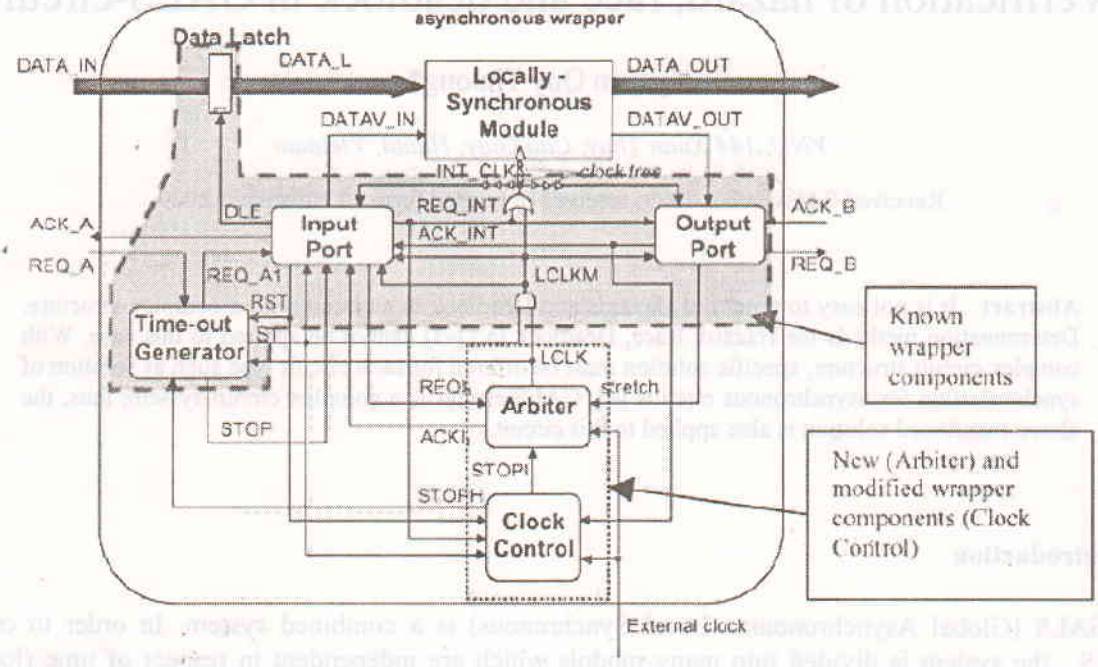

Fig. 2. GALS wrapper with external clocksource.

It should be confirmed that circuits of wrappers must suit their special properties and especially during working time not creating hazards which might affect working regime of wrappers. Of course, it is impossible to determine all hazards in a circuit by incomplex tests. Checking a circuit can only point out the presence of mistakes but cannot change them. In order to ensure the accurate operation of a system of GALS, it is necessary to verification asynchronous circuits during design process and changes of hazards, deadlocks and signal race. Achieved results will be included in circuit design. Wrapper will be restructured and verification for substitution.

2. Removal of hazard, race and deadlocks from GALS - circuit

Petrinets describe a display mean for race of different signals and be popular formalismus for modellizing asynchronous circuits. There are two different starting points: modelling of level and impulse flank. In impulse flank use, special properties of a asynchronous circuit are described as Signal Transition Graph, STG. STGs is a special type of Petrinets and their transitionen is described by impulse flank. Circuit of a transition is modelled in suitability with effect of a impulse flank in a asynchronous circuit. This model requires strictness for changes of transitions of a signal. In level based use, a binary signal is modelled by 2 positions (Signallevel 0 and 1). A mark is in correspondence with a level of signal. Circuit of a transition describes a change of a signal. On the contrary, a symbol in use based on impulse flank is not modelled following level but following change of a impulse flank of a signal as well as change of signal level. Using following impulse flank is more suitable than other models to simulate circuit elements like XOR, or Mueler – C while level model is used to simulate AND and OR gates.

In order to analyze properties of Deadlock and Hazard in Petrinets of wrappers, for each gate type, there will be a petrinetsample. This type ensures all necessary information for detecting a hazard in the circuit. After all transitions of a closed petrinetsample, from its distribution place, more than one mark will be created to suit level change of two input signals. This level occurs in a very short period. If it occurs at a gate, two input signals will simultaneously changes their values and corresponding gate in circuit can create hazards [2]. Joint wrapper model is created from an constitution of a petrinetsample which suits list of gattnet.

After having a mark, a model check set by LoLA (Low Level Analyse) can be used. LoLA checks an available model as a petrinet with temporary properties, in which, this transition system is organized and analysed. In here, LoLA uses the technique of reducing big capacity to avoid explosion. Therefore, status space which needs to be surveyed can be limited. For each gate of circuit, hazards at output points shall be determined if they are available or not.

Of course, this reducing technique which is applied in case of models is not enough to limit the status space. Thus, we may use the method of abstraction. The aim of this method is to make the transition system small but not lose properties which need to be controlled. Wrapper model is divided into n elements. Each element will combines with an abstracted area (abstraction of all n different - 1 element) to create a model. The concept is to only survey hazards at all gates in a element. This element is available as a concrete petrinetsample in a abstract adjacent area. Abstact adjacent area comprises of abstraction following step by step method which is describe by imitative relation between concrete model and abstract model. Imitation is a relation which is described by mathematics, presenting the relation of concrete system an abstract system.

With more carefully survey, LoLA can determine routes with fault in the transition system. This route is considered as a set to translate preceding data into corresponding rows of signals. In wrapper circuit, this row of signals will be checked. If there is actually any hazard, selected structures of circuit must be found out.

Based on analysis results, the circuit will be newly structured to create proper time ties. Logical connection of gates will be restructured until the circuit is suitable with desired relations.

After that, models are continuously surveyed by LoLA. These processes will be repeated until there is no fault in working mode of the circuit. Following this method, hazard, signal race and deadlock in wrapper can be wiped out. If our assumptions are correct, there will be no fault in the circuit.

3. Conclusion

Depend on Petrinets combine with a model check set by LoLA, status space hazard, race, deadlock which needs to be surveyed can be limited, to say this method is to make the transition system small but not lose properties which need to be controlled. This time Wrapper model is divided into n small elements. Each element will combines with an abstracted area . This combine which is describe by imitative relation between concrete model and abstract model. From here we have determine routes with fault in the transition system. These processes will be repeated until there is no fault in working mode of the circuit. Obvious to verification hazard, race, deadlock in GALS then can not use this methods Karnaugh map, circuit and Booleal algebra, matrix methode.

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