Using high algebra to design frequency divider include hazard

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Abstract. Normally the frequency divider designed by Boole algebra and to design a frequency divider with any divide factor, we have to repeat all over again every design step as the same. So to avoid of wasting time and money, instead of using traditional Boole algebra in digital technical we replace it by mathematical models in high algebra. And because of that we can design frequency dividers use computer.

1. Modeling of function circuit

Follow [1,2] show that with one frequency divider has 4/3 factor we need 2 flip flop (FF) and NAND gates to control chain so that with 4 input impulse we just have only 3 output impulse. However using NAND gate to control output impulse likes this, it just right in some cases. So to design frequency divider with any divider K factor (meaning with any input and output impulse follow request of user) we use OR gate to control output impulse.

Investigate, for example, the input static D and output static Q of D FF in asynchronous Divider, real binary, 3 input, divide factor K= 7/6)
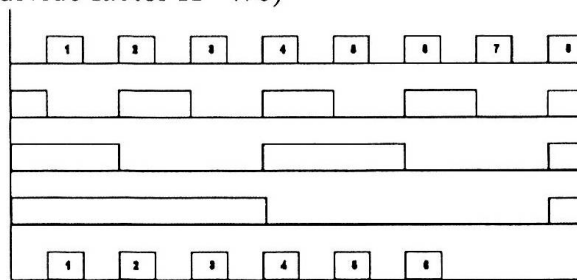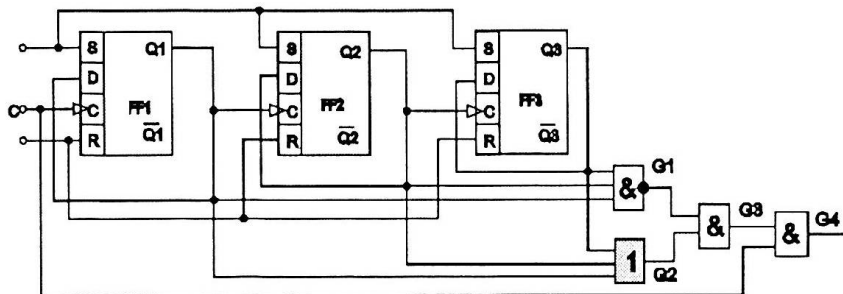

Fig 1. Diagram impulse of frequency divider 7/6.

Fig. 2. Frequency divider 7/6 execute follow diagram impulse Fig. 1.

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From circuit of frequency divider picture 2 and impulse diagram Fig. 1, we realize that in the time of first impulse to sixth impulse have at lease one of three input signal of NAND gate G1 receive 0, so output of G3 {G1,G2} $\hat{=} 1$. In this time frequency divider will receive 6 impulses from output gate G4. To impulse 7 output of gate G2 {Q1, Q2, Q3} receive level 0 and because of that G3 $\hat{=} 0$, follow G4 receive level 0 too. So because of OR gate G2, we controlled output frequency divider is M = 6.

From Fig. 2 we have circuit function of frequency divider 7/6

$$K = \frac{7}{6} \hat{=} \overline{Q_1 Q_2 Q_3} (Q_1 + Q_2 + Q_3).C \tag{1}$$

If frequency divider has $K = \frac{x}{6}$ with any x input impulse, mean any n Flip Flop , example 8/6, 9/6, ...x/6 then discover more output Q_4, Q_5 ....of FF4, FF5... from OR input. Now frequency divider with $K = \frac{x}{6}$ have circuit function:

$$K = \frac{7}{6} \hat{=} \overline{Q_1 Q_2 Q_3} (Q_1 + Q_2 + Q_3).Q_4 Q_4 ...C \tag{2}$$

Obvious, because of OR gates then after output impulse position M, circuit will reset.

Same as above we have Table 1, x is number of input impulse, M is number output impulse and K is a divider factor.

Table 1. Circuit function of frequency divider with any divide factor $K = \frac{x}{M}$, x is number of input impulse,

M is number output impulse, here $M \in [4,31]$

$K = \dfrac{x}{M}$	Function
$x/4$	$\overline{Q_1 Q_2 Q_3} (Q_1 Q_2 + Q_3) Q_4$
$x/5$	$\overline{Q_1 Q_2 Q_3} (Q_2 + Q_3) Q_4$
$x/6$	$\overline{Q_1 Q_2 Q_3} (Q_1 + Q_2 + Q_3) Q_4$
$x/7$	$\overline{Q_1 Q_2 Q_3 Q_4}$
$x/8$	$\overline{Q_1 Q_2 Q_3 Q_4} (Q_1 Q_2 Q_3 + Q_4) Q_5$
$x/9$	$\overline{Q_1 Q_2 Q_3 Q_4} (Q_2 Q_3 + Q_4) Q_5$
$x/10$	$\overline{Q_1 Q_2 Q_3 Q_4} [(Q_1 + Q_2) Q_3 + Q_4] Q_5$
$x/11$	$\overline{Q_1 Q_2 Q_3 Q_4} (Q_3 + Q_4) Q_5$
$x/12$	$\overline{Q_1 Q_2 Q_3 Q_4} (Q_1 Q_2 + Q_4) Q_5$
$x/13$	$\overline{Q_1 Q_2 Q_3 Q_4} (Q_2 + Q_3 + Q_4) Q_5$
$x/14$	$\overline{Q_1 Q_2 Q_3 Q_4} (Q_1 + Q_2 + Q_3 + Q_4) Q_5$
$x/15$	$\overline{Q_1 Q_2 Q_3 Q_5}$
$x/16$	$\overline{Q_1 Q_2 Q_3 Q_4 Q_5} (Q_1 Q_2 Q_3 Q_4 + Q_5) Q_6$
$x/17$	$\overline{Q_1 Q_2 Q_3 Q_4 Q_5} (Q_2 Q_3 Q_4 + Q_5) Q_6$
$x/18$	$\overline{Q_1 Q_2 Q_3 Q_4 Q_5} [(Q_1 + Q_2) Q_3 Q_4 + Q_5] Q_6$

$x/16 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_1Q_2Q_3Q_4 + Q_5)Q_6$

$x/17 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_2Q_3Q_4 + Q_5)Q_6$

$x/18 \quad \overline{Q_1Q_2Q_3Q_4Q_5}[(Q_1 + Q_2)Q_3Q_4 + Q_5]Q_6$

$x/19 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_3Q_4 + Q_5)Q_6$

$x/20 \quad \overline{Q_1Q_2Q_3Q_4Q_5}[(Q_1Q_2 + Q_3)Q_4 + Q_5]Q_6$

$x/21 \quad \overline{Q_1Q_2Q_3Q_4Q_5}[(Q_2 + Q_3)Q_4 + Q_5]Q_6$

$x/22 \quad \overline{Q_1Q_2Q_3Q_4Q_5}[(Q_1 + Q_2 + Q_3)Q_4 + Q_5]Q_6$

$x/23 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_4 + Q_5)Q_6$

$x/24 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_1Q_2Q_3Q_4 + Q_5)$

$x/25 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_2Q_3 + Q_4 + Q_5)Q_6$

$x/26 \quad \overline{Q_1Q_2Q_3Q_4Q_5}[(Q_1 + Q_2)Q_3 + Q_4 + Q_5]Q_6$

$x/27 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_3 + Q_4 + Q_5)Q_6$

$x/28 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_1Q_2 + Q_3 + Q_4 + Q_5)Q_6$

$x/29 \quad \overline{Q_1Q_2Q_3Q_4Q_5}(Q_2 + Q_3)Q_4 + Q_5)Q_6$

$x/30 \quad \overline{Q_1Q_2Q_3Q_4Q_5}[(Q_1 + Q_2 + Q_3 + Q_4 + Q_5)]Q_6$

$x/31 \quad \overline{Q_1Q_2Q_3Q_4Q_5Q_6}$

From table 1 and comment above, we realize circuit function of frequency divider with any divider factor have 2 forms:

form 1:
$$K_n^1 = \overline{Q_1Q_2...Q_{n-1}} \cdot Q_n = \overline{\prod_{i=1}^{n-1}Q_i..Q_n}$$
(3)

A part of function left over in brackets (Table1) is a second form :

form 2:
$$K_n^2 = y + Q_n$$
(4)

We need to define function y.

2. Define y of circuit function

From circuit function (Table 1) we found the form 2 (Table 2)

Table 2. Circuit function form 2 apply to frequency divider with divide factor $K = \dfrac{x}{M}$, n is number of Flipflop, F is frequency appear circuit function in proportion to K factor, $F_b \in |\ 0,1,2,3\ |$ is a basic frequency to show circulate of circuit function

Flipflop n	Basis frequenz F_B	Frequenz F	K = x/M	Form 2
	0	0	x/4	$Q_1 Q_2$ $+ Q_3$
	1	1	x/5	Q_2 $+ Q_3$
	2	2	x/6	$Q_1 + Q_2$ $+ Q_3$
3	3	3	x/7	1 $+ Q_3$
4	0	0	x/8	$Q_1 Q_2$ $.Q_3 + Q_4$
	1	1	x/9	Q_2 $Q_3 + Q_4$
	2	2	x/10	$(Q_1 + Q_2)$ $.Q_3 + Q_4$
	3	3	x/11	1 $.Q_3 + Q_4$
	0	4	x/12	$Q_1 Q_2$ $+ Q_3 + Q_4$
	1	5	x/13	Q_2 $+ Q_3 + Q_4$
	2	6	x/14	$Q_1 + Q_2$ $+ Q_3 + Q_4$
	3	7	x/15	1 $+ Q_3 + Q_4$
	0	0	x/16	$Q_1 Q_2$ $.Q_3 Q_4 + Q_5$
	1	1	x/17	Q_2 $.Q_3 Q_4 + Q_5$
	2	2	x/18	$(Q_1 + Q_2)$ $.Q_3 Q_4 + Q_5$
	3	3	x/19	1 $.Q_3 Q_4 + Q_5$
	0	4	x/20	$(Q_1 Q_2$ $+ Q_3) Q_4 + Q_5$
	1	5	x/21	$(Q_2$ $+ Q_3) Q_4 + Q_5$
	2	6	x/22	$(Q_1 + Q_2$ $+ Q_3) Q_4 + Q_5$
	3	7	x/23	$(1$ $+ Q_3) Q_4 + Q_5$
	0	8	x/24	$Q_1 Q_2$ $. Q_3 + Q_4 + Q_5$
5	1	9	x/25	Q_2 $. Q_3 + Q_4 + Q_5$
	2	10	x/26	$(Q_1 + Q_2)$ $. Q_3 + Q_4 + Q_5$
	3	11	x/27	1 $. Q_3 + Q_4 + Q_5$
	0	12	x/28	$Q_1 Q_2$ $+ Q_3 + Q_4 + Q_5$
	1	13	x/29	Q_2 $+ Q_3 + Q_4 + Q_5$
	2	14	x/30	$Q_1 + Q_2$ $+ Q_3 + Q_4 + Q_5$
	3	15	x/31	1 $+ Q_3 + Q_4 + Q_5$

From table 2 we realize: circuit function need to find matching with each divide K factor depend on n and F, also we can build the relationship between n, F, M

$$M = 4.2^{n-3} + F \qquad (5)$$

$$F = M - 4.2^{n-3} \qquad (6)$$

Provide: - n is a number of Flipflop take parts of divider.

- F is frequency appear of circuit function in each frequency divider n- FF, follow one circulate from 0 to 2^n - 1

Also from table 2 we realize a part of circuit function of frequency divider having output impulse M from 4 to 7 (in proportion to n = 3, F = (0, 1, 2, 3)) is just a part of circuit function have output impulse M ≥ 8 (this is Q_1Q_2 ; Q_2 ; $Q_1 + Q_2$; 1). So we take this circuit function make a basic form and symbol as $y_{n=3}$ to define circuit function of all other frequency divider:

$$y_{n=3}(A_1, A_2) = \begin{cases} A_1 & if \ F = \left[0, \ 2^{n-2} -1\right] \\ A_2 & if \ F = \left[2^{n-2}, \ 2^{n-1} -1\right] \end{cases} \qquad (7)$$

In which:

$$A_1 = (Q_1 + \xi) \cdot Q_2 \qquad with \ \xi = \begin{cases} 0 & if \ F = 0 \\ 1 & if \ F = 2^{n-2} -1 \end{cases} \qquad (8)$$

It call Product Form

$$A_2 = (Q_1 + \xi) + Q_2 \qquad with \ \xi = \begin{cases} 0 & if \ F = 2^{n-2} \\ 1 & if \ F = 2^{n-1} -1 \end{cases} \qquad (9)$$

It call Sum Form

From (8) and (9) and consider $Q_1 + \xi = A_\xi$ we have:

$$y_{n=3} = (Q_2 + \beta)A_\xi + \beta Q_2 \qquad (10)$$

In which:

$$\beta = \begin{cases} 0 & if \ F = \left[0, \ 2^{n-2} -1\right] \\ 1 & if \ F = \left[2^{n-2}, \ 2^{n-1} -1\right] \end{cases} \qquad (11)$$

Thus:

$$K^2_{n=3} = y_{n=3} + Q_3 \qquad (12)$$

From table 2 show that circuit function in proportion to n = 4, when Frequency $F_b = (0,...3) = [0, ..., 2^{n-2} -1]$ then circuit function has also product form and sum form as $y_{n=3}$ and this circuit function include circuit function of $y_{n=3}$. We call this circuit function form is $y_{n=4}$

Thus

$$y_{n=4} = (Q_3 + \psi)y_{n=3} + \psi Q_3 \qquad (13)$$

In which:

$$\psi = \begin{cases} 0 & if \ F = \left[0, \ 2^{n-2} -1\right] \\ 1 & if \ F = \left[2^{n-2}, \ 2^{n-1} -1\right] \end{cases} \qquad (14)$$

Thus:

$$K^2_{n=4} = y_{n=4} + Q_4 \qquad (15)$$

Same as let n = 5 with $F_b = (0,...7) = [0, ..., 2^{n-2} -1]$ and n = 6 with $F_b = (0,...15) = [0, ..., 2^{n-2} -1]$

Thus:

$$y_{n=5} = (Q_4 + \lambda)y_{n=4} + \lambda Q_4 \qquad (16)$$

with:

$$\lambda = \begin{cases} 0 & if \ F = \left[0, \ 2^{n-2} -1\right] \\ 1 & if \ F = \left[2^{n-2}, \ 2^{n-1} -1\right] \end{cases} \qquad (17)$$

Thus:
$$K^2_{n=5} = y_{n=5} + Q_5 \tag{18}$$

and:
$$y_{n=6} = (Q_5 + \theta)y_{n=5} + \theta Q_5 \tag{19}$$

with
$$\theta = \begin{cases} 0 & if \quad F = \left[0,\ 2^{n-2} - 1\right] \\ 1 & if \quad F = \left[2^{n-2},\ 2^{n-1} - 1\right] \end{cases} \tag{20}$$

$$K^2_{n=6} = y_{n=6} + Q_6 \tag{21}$$

3. The existence of circuit functions follows a certain law

From a result above we realize circuit function to n = 6 follow a certain law with repeat periode F_b= [0, 2^{n-2} -1], a problem now is how to prove with variable intput n > 6 and any value then circuit function follow a certain law when n ≤ 6 or not.

Assuming that $f(M) = K_n$ is a function satisfying term Dirichlet of Fourier [3] theorem on period [0, 2^{n-2} - 1] = [a,b]. In order to develop f(M) into Fourier series, we form a periodic function g(F_b) having a period either bigger or equal to [b – a] so that

$$g(F_b) = f(M) \quad \forall F_b \in [a,b] \triangleq \left[0, 2^{n-2} - 1\right] \tag{22}$$

Obviously there are many ways to develop g(F_b) into Fourier series. For each g(F_b) there are corresponding Fourier series, therefore there are a number of Fourier series demonstrating f(M) = K_n, in other words, the circuit function f(M) = K_n with every M is periodicall with period ΔF_b= 2^{n-2} – 1, in here ΔF_b Determine from table 2.

From demonstration above, we realize that circuit function depend on ΔF_b = [0, 2^{n-2} -1]. With circuit functions in proportion to Fb $\notin$ [0, 2^{n-2} -1] then we have to change F to Fb. so to determine of circuit function we need to find the value F_b. From table 2 we have:

$$F_b = F - 4.(n - 3) \tag{23}$$

Now that we can assert that with any variable input n, that is the frenquency divider can (theoretically) divide to infinite number, then the impulse diagram of circuit function change periodically in those periods which have similar impulses, that is circuit functions always have form 1 and 2 according to certain ΔF

To here, we define that circuit function of frequency divider is change periodically follow a certain circulate, in other words, circuit function in any form K_{n-3}, K_{n-4}, K_{n-5}, K_{n-6}, ... have same form apply with same F frequency. From (11) to (18) we can define of 2 comprehensive forms of circuit function of one frequency divider with output impulse and input as we expect:

$$K^2_n = (Q_{n-1} + \varphi).f_n(y) + \varphi.Q_{n-1} + Q_n \tag{24}$$

With
$$\varphi = |\beta, \psi, \theta, \lambda| = \begin{cases} 0 & if \quad F = \left[0, 2^{n-2} - 1\right] \\ 1 & if \quad F = \left[2^{n-2},\ 2^{n-1} - 1\right] \end{cases} \tag{25}$$

$$f_n(y) = \begin{cases} y_n = f(y_{n-1}) \\ y_{n-1} = f(y_{n-2}) \\ \dots \\ y_4 = f(y_3) \end{cases} \tag{26}$$

Combine form 1 and 2 we realize that circuit function of frequency divider correspondence with any number of input impulse and number of output impulse expect:

$$K_n = \left| K_n^1 + K_n^2 \right| \tag{27}$$

$$K_n = \overline{\prod_1^n Q_i[(Q_{n-1} + \varphi).f_n(y) + \varphi.Q_{n-1} + Q_n].Q_{n+1}} \tag{28}$$

Provide: - n is a number of FF participate in frequency divider
  - φ is show as function (25)
  - $f_n(y)$ is show as function (26)
  - K_n, K_{n-1},... K_4, K_3 are circuit function corresponding to different n

4. Determine hazard of circuit function

From circuit function (28) we can see output state Q of Fflipflop in negative $(\overline{Q})$ and not negative Q. Follow [4,5] when have same output in negative form and not negative form then a chance to create hazard is big, so we need to Determinated that circuit stay in one of static – 0 hazard $\overline{x}x$ (Fig.3a), static-1 hazard $x + \overline{x}$ (Fig 3b), dynamic hazard $\overline{x}x + x$, $(x + \overline{x})x$ (Fig.3c,d) or not.
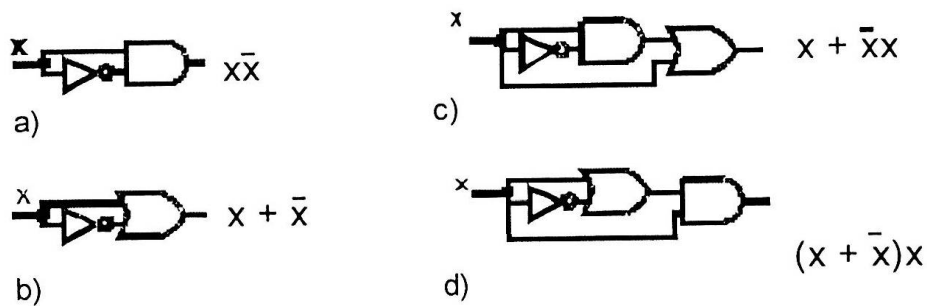

Fig. 3. Basis hazards.

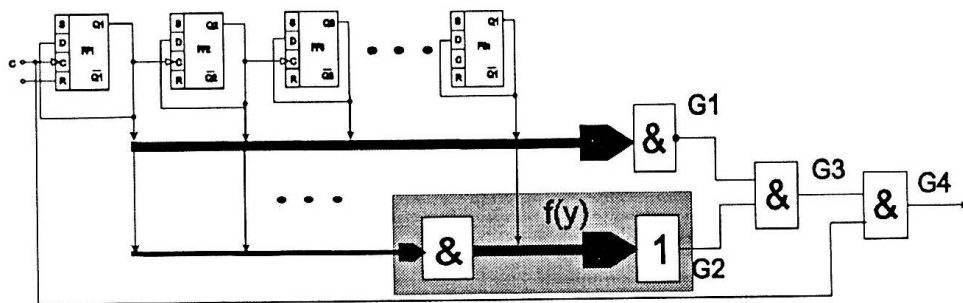From function (28) we can build comprehensive circuit of frequency divider:

Fig. 4. Comprehensive circuit of frequency divider.

From comprehensive circuit we can construct the residual circuit.
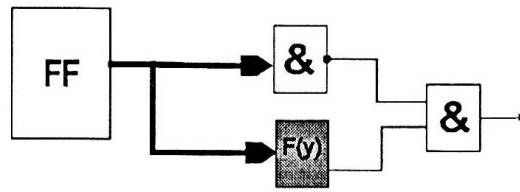
Shown in Fig. 5:

Fig. 5. The residual circuit of frequency divider.

Compare residual circuit of frequency divider (Fig 5) with circuit showing basic hazards (Fig.3), we realize circuits of basic hazards where $\overline{x}$ and x stay in two different flat surface algorithm and connected series (Fig. 6b). It will appear delay in surface $\overline{x}$ before come to surface x, this is cause of hazard. On the contrary, with frequency divider $\overline{x}$ and x also stay in one surface algorithm (Fig. 6a), they are "equal" on another, so it not delay circuit $\overline{x}$ to appear hazard. In other word, the frequency divider showing in (28) is free hazard.

a)   b)
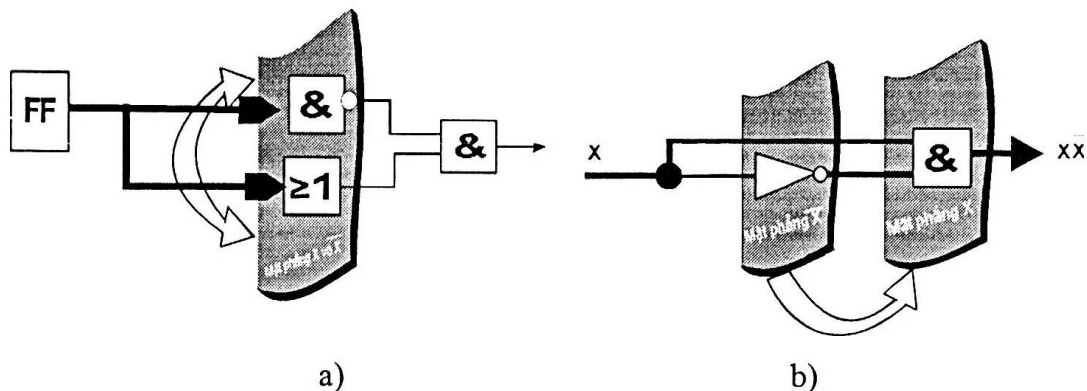
Fig. 6. Illustration that frequecy divider is free Hazard.

So because of function (28) we design frequency divider with Matlab software without using Boole algebra. From that we can design frequency divider with any divider factor K using computer, and free hazard in circuit function.

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