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Original Article

Demonstration on Ferroelectric-gate Thin Film Transistor NAND-type Array with Disturbance-free Operation

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Abstract: A novel concept of NAND memory array has been proposed by using only ferroelectric-gate thin film transistors (FGTs), whose structure is constructed from a sol-gel ITO channel and a sol-gel stacked ferroelectric between $Bi_{3.25}La_{0.75}Ti_3O_{12}$ and $PbZr_{0.52}TiO_{0.48}O_3$ (BLT/PZT) gate insulator. Interestingly, ferroelectric cells with a wide memory window of 3 V and a large on/off current ratio of 6 orders, have been successfully integrated in a NAND memory circuit. To protect data writing or reading from disturbance, ferroelectric transistor cells are directly used, instead of paraelectric transistor cells as usual. As a result, we have verified disturbance-free operation for data reading and writing, with a small loss of the memory state and a low power consumption, in principle.

Keywords: ITO, PZT, NAND, FeRAM, ferroelectric.

1. Introduction

Due to nature of ferroelectric materials, of which the polarization is able to be switched in nano-second order, very recently, their memorizable functions have been characterized in depth as a promising candidate of non-volatile memory generation [1-4]. In parallel, bismuth ferrite, $BiFeO_3$ (BFO), brings a motivating challenge for ferroelectric memory application, owing to its high remnant polarization [5, 6]. Unfortunately, a leakage current is considerably existed in BFO, which makes the memory function to be degraded [7]. On the other hand, it has been well known that traditional ferroelectric materials such as $SrBi_2Ta_2O_9$ (SBT), $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT), and $PbZr_{0.52}TiO_{0.48}O_3$ (PZT) are really attractive in electronic devices application. For instance, SBT thin films possess a low leakage current but a small remnant polarization and high crystallization temperature [8], PZT thin films have a large remnant

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polarization and lower crystallization temperature, but a large leakage current [9, 10]. As a trade-off material, BLT thin films involve a medium level of leakage current, remnant polarization and crystallization temperature between SBT and PZT thin films [11]. These properties make BLT thin films to become an expected option for the practical use.

Thin film transistor NAND-type flash memory and NAND-type memory array with Metal-Ferroelectric-Insulator-Semiconductor structure have been reported with good data retention and endurance [12, 13]. However, the data-disturbance, especially the signal loss of the OFF state in the unselected cell (UC), is a serious issue when reading the stored data of the selected cell (SC) in any conventional NAND-type memories. To overcome this difficulty, NAND EEPROMs using a side-wall transfer-transistor cell has been reported, in which the Si-based transfer transistor was used to protect data of the UC. Also, in order to solve the data-disturbance essentially, Panasonic Corporation has developed a NAND model based on mostly epitaxial growth technique to archive a data disturbance-free operation [14].

As reported previously, we succeeded to demonstrate an adequate operation of a ferroelectric-gate thin film transistor (FGT), whose channel and gate insulator are derived from a solution process [15, 16]. Based on these results above we attempt to propose a NAND array using only FGTs. That would lead to a low-cost nonvolatile memory in future. In this work, we demonstrate data disturbance-free operation of the FGT-NAND array which uses a sol-gel ITO channel and sol-gel stacked (BLT/PZT) gate insulator.

2. Non-disturbance operation principle

Figure 1(a) shows the schematic of FGT-NAND array, where each FGT structure is shown in its inserted figure. Each cell consists of two FGTs, whose sources and drains are connected to each other. Here, one FGT (m-Tr: memory transistor) is to store data, and the other (p-Tr: pass transistor) is to protect data from disturbance, that is, a pass line (PL) can be electrically formed into FGT-NAND. The write/read operation of FGT-NAND is described as follows:

Data-write the C12 (Fig. 1(b))

- Word line (WL2) of the selected C12 is applied at ±6 V. Other WLs and PLs are kept even at 0 V to turn ON p-Trs. This is due to ferroelectric-gate nature of FGTs.

- Bit line (BL1) is 0 V, other BLs are applied at the same voltage with WL2. By this action, the data can be written only on the selected C12.

b. Data-read the C12 with disturbance-free (Fig.1(c))

All WLs and PLs are grounded because p-Trs can keep ON even at 0 V as mentioned above.

BL1 is biased by a voltage swept from 0 to 0.3 V, while other BLs are grounded.

PL2 is first applied by a negative pulse to turn OFF p-Tr (C12) while other TLs are 0 V to keep ON the other p-Trs, so that the stored data of m-Tr (C12) can be decoded. After that, PL2 is followed by a positive pulse to turn ON p-Tr (C12) again for protection of the m-Tr (C12) continuously. By this action, we can always decode the stored data of the SC, but not disturb the data of UCs regardless of their memory states.

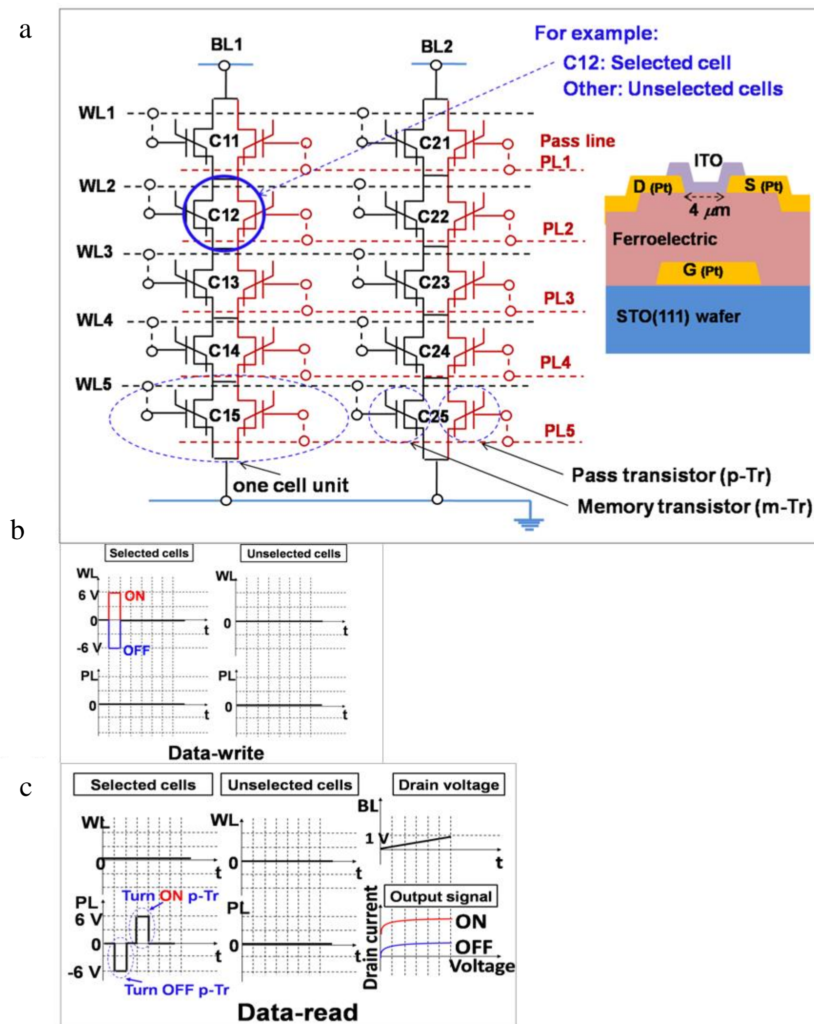


Figure 1. (a) FGT-NAND array for data disturbance-free, (b) voltages applied for data-write of the FGT-NAND array, and (c) voltages applied for data-reading to ensure disturbance-free of the FGT-NAND array.

3. FGT-NAND array fabrication

Figure 2(a) shows a top-view of the FGT-NAND fabricated with ten FGTs, and Fig. 2(b) shows a cross section of either A-B or C-D line. Equivalent circuit of the fabricated FGT-NAND array is corresponded to the first unit of Fig. 1(a). For the device fabrication, first, a Pt bottom gate was fabricated by sputtering. Second, a new stacked 20-nm-thick BLT/160-nm-thick PZT film was prepared by sol-gel method. Here, the BLT layer prevents diffusion of Pb from the PZT film and creates a well-formed interface with the channel. Third, a Pt film was deposited as the source and the drain electrodes by sputtering. Finally, a 20-nm-thick ITO channel was formed by sol-gel method. The channel length (L), channel width (W) and gate length (L_G) of each FGT were 4, 60 and 50 μm, respectively. Detailed technique can be found in our previous work [16].

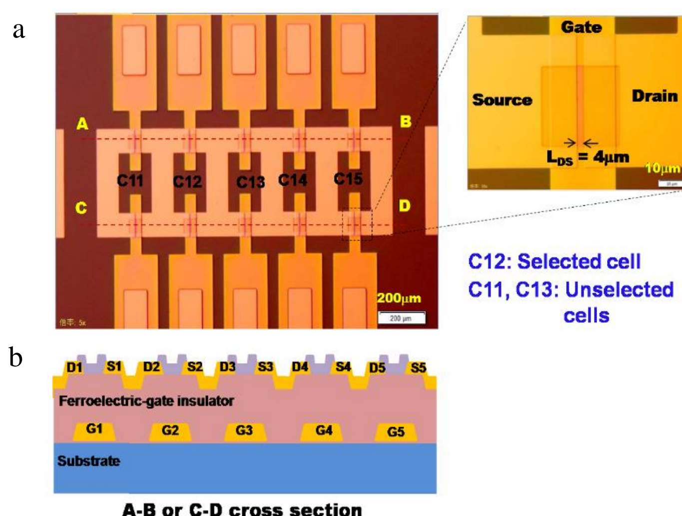


Figure 2. (a) Top-view of the fabricated FGT-NAND array, (b) cross-section view of either A-B or C-D line.

4. Results and discussion

Figure 3(a) shows the transfer characteristic (I_D-V_G) where the gate voltage V_G was doubly swept from -7 to 7 V at a constant drain voltage V_D of 0.3 V. This characteristic is relatively equivalent with nano-sized FGT, if the memory cell is scaled down further [15], and it is comparable with a vacuum process of ITO thin film with BLT gate insulator [17]. Hereafter, it is interesting that when both m-FGT and p-FGT are operated together, their I_D-V_G curve behaves as the black curve (case 1), where it shows a memory window of 3 V and ON/OFF ratio of 10^6. If we turn ON p-FGT while measuring the I_D-V_G of m-FGT, its behavior likes the red curve, that is, the circuit is shorten (case 2). On the other hand, if we turn OFF p-FGT while measuring the I_D-V_G of m-FGT, its behavior likes the blue curve, that is similar to that shown in black curve (case 3). This result implies that the p-Tr can protect or pass the stored signal of the m-FGT smoothly. Figure 3 (b) shows the output characteristic (I_D-V_D) of each cell. The V_D was swept from 0 to 15 V, while the V_G was also increased from 0 to 8 V with a step of 1 V. We can see that a well-saturated behavior and a large ON saturation current could be obtained by using this FGT-NAND.

Although the retention time is not shown here, we verified that it is extended to several hours which are adequate to evaluate data-disturbance. For this purpose, we investigated on three cells (e.g., C12: selected, C11 and C13: unselected), as shown in Fig. 2(a), and followed an operation sequence as shown in Fig. 4(a). For data-write, we applied voltages shown in Fig. 1(b) to FGT-NAND. For data-read, we applied voltages shown in Fig. 1(c) to FGT-NAND.

When the FGT-NAND cell is ON, its drain current is ON-level. On the contrary, when the FGT-NAND cell is OFF, its drain current is OFF-level as shown in Fig. 4 (b). They are almost 6-order difference between ON state and OFF state as can be also seen from Fig. 3 (a). Note in Fig. 4 (a) that, when writing and reading data of the selected C12, m-Tr1 of the unselected C11 was OFF and p-Tr1 of the unselected C11 was ON. So, we checked the p-Tr1 could protect the OFF state of m-Tr1 or not. Figure 4(b) shows that the OFF state in m-Tr1 of the unselected C11 is slightly disturbed owing to a little bit higher than OFF-level, after data write/read of the selected C12. However, it is acceptable for

this change by considering some discharge in each FGT. We confide that further size reduction of the overlap area between the gate and source-drain electrodes and improvement of each film layer could bring us better disturbance-free property. One noted that the p-Tr1 is able to operate even connecting its gate with the ground, which is different from another work using paraelectric transistor [14]. That is, the proposed NAND structure would support strongly to a lower consumption, and non-volatile function.

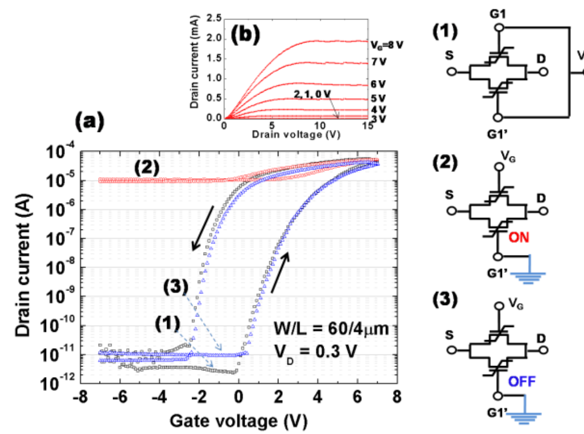
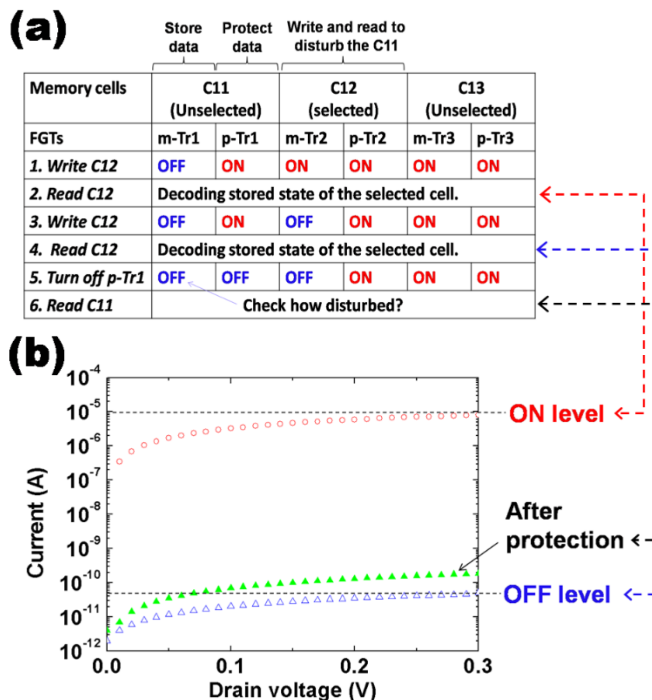


Figure 3. (a) Transfer characteristics of one cell while: (case 1) both FGTs operate, (case 2) p-FGT is ON, and (case 3) p-FGT is OFF; and (b) output characteristics corresponded to the case 1.


(a)

	Store data	Protect data	Write and read to disturb the C11			
Memory cells	C11 (Unselected)		C12 (selected)		C13 (Unselected)	
FGTs	m-Tr1	p-Tr1	m-Tr2	p-Tr2	m-Tr3	p-Tr3
1. Write C12	OFF	ON	ON	ON	ON	ON
2. Read C12	Decoding stored state of the selected cell.					
3. Write C12	OFF	ON	OFF	ON	ON	ON
4. Read C12	Decoding stored state of the selected cell.					
5. Turn off p-Tr1	OFF	OFF	OFF	ON	ON	ON
6. Read C11	Check how disturbed?					

Figure 4. (a) A sequence to verify a data disturbance-free of FGT-NAND, and (b) disturbance-free confirmation of the FGT- NAND array.

5. Conclusion

A FGT-NAND memory array was successfully designed and demonstrated using only ferroelectric-gate thin film transistors with solution-processed channel and gate insulator. A wide memory window (3V) and a large on/off current ratio (10^6) were obtained for each cell. In consequence, the big issue on the data-disturbance of the conventional NAND circuit was solved with a small loss of the stored signal. This result gives us a great challenge to make further size-downing to satisfy a logic circuit application in future.

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