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Original Article

Fabricating Ultra-thin Silicon Nitride Membranes Suspended on Silicon Wafer

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Abstract: Ultrathin silicon nitride SiNx membrane suspended on a silicon wafer is a popular two-dimensional platform in MEMS applications. The unsupported membrane has a low thermal conductivity, is electrically insulated, and very robust against mechanical impact. Remarkably thin, it is difficult to fabricate and manipulate. Recently equipped with a dual chamber system for plasma enhanced chemical vapor deposition (PECVD) and reactive ion etching, we calibrate it to deposit silicon nitride Si3N4, silicon dioxide SiO2, and to dry etch these materials. Based on the superb quality of Si3N4, we perform a through-wafer etch that creates suspended Si3N4 membranes. The recipe is reliable and reproducible. We analyze the membrane's chemical composition and optical properties. Although created by PECVD, the membrane is so robust that it survives multiple lithography steps. It extends our capability to study thermal transport at the submicron scale as well as to fabricate micron size devices for MEMS applications.

Keywords: Power MEMS, Silicon nitride membranes, PECVD, silicon wafer.

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1. Introduction

Micro-Electro-Mechanical Systems (MEMS) often require qualities that a traditional silicon wafer can not meet. For example, in thermoelectric applications, the cold part of a micro-refrigerator should be isolated from the environment, while the hot part should stay thermalized with the surrounding. A platform that separates two regions of different thermal conductance is vital for the device performance [1-3]. Silicon nitride membranes have low stress, low thermal conductance, are electrically isolated, and thus, are an ideal platform for such applications. It is the best platform to study thermal transport at the submicron scale [4-7]. Not limited to micro-cooling applications, the membrane is transparent under the high energy electron beam and is widely used in the transmission electron microscopy community [8]. The same recipe to fabricate the membrane can also be employed to fabricate other structures [9], such as pressure sensors [10], RF switches [11], or atomic force microscope cantilevers [12].

Extremely fragile, only certain labs possess the capability to fabricate suspended membranes. There are two main challenges. First, the high aspect ratio: 100 nm thin and a millimeter square suspended area make it so fragile that the yield becomes very low, which requires a low-stress material. Second, through-wafer etching is a demanding process that needs a long etching time in corrosive chemical solutions. The deposited dielectric thin film should be strong enough to survive such a process. Among dielectric materials, Si_3N_4 is the traditional choice due to its high quality as a low-stress material [13] and its compatibility with nano-fabrication processes.

Silicon nitride SiN_x and silicon oxide SiO_x are the two most important dielectric materials to use with silicon wafers. They can be used as passivation layers, isolating films, or piezoelectric materials, to name a few. They are mostly created from Chemical Vapor Deposition (CVD) method, with quality depends on the detail approaches: plasma enhanced CVD, low pressure CVD, hot wire CVD, or atomic layer deposition. Among these approaches, low pressure chemical vapor deposition (LPCVD) produces Si_3N_4 of high purity, low stress, and low price and can be used for mass production [14, 15]. However, it requires a high temperature and would destroy any pre-existed structure on the wafer. Depositing Si_3N_4 using LPCVD has to be the first step of the fabrication, which limits the popularity of the method. To lower such temperature barrier, the deposition in a plasma enhanced chemical vapor deposition (PECVD) machine occurs with the help of a plasma environment [16, 17]. The depositing temperature is often below 400 ℃ and is compatible with a wide range of processes. The lower temperature, however, alters the quality of SiN_x films, including their stoichiometry [18]. As a result, it is a challenge to fabricate suspended membrane using Si_3N_4 deposited using PECVD. It is important to have a correct recipe that produces Si_3N_4.

Recently, we are equipped with a dual plasma chamber system that can both dry etch and deposit in the two adjacent vacuum chambers, connected with a load-lock. We report a recipe that fabricates ultrathin silicon nitride membrane using such system, where the Si_3N_4 is deposited in the PECVD chamber, and subsequently an etching window is opened in the reactive ion etching (RIE) chamber. The film is deposited using silane SiH_4 and ammonia NH_3, while the Si_3N_4 is etched with SF_6. Both deposition and etching conditions are carefully analyzed. The SiN_x bandgap is measured using ellipsometry technique [19]. We adjust the deposition parameter according to this measurement. The chemical etch rate is measured using a profilometer. The suspended membrane is then released using a through wafer wet-etching in KOH. The thin film is atomically flat with the stoichiometry ratio Si/N at 0.75. It is important to emphasize that even with the low quality of Si_3N_4 produced by a PECVD machine, the membrane is mechanically robust. It survives multiple lithography steps including wet etches and metal depositions. The recipe is reliable and reproducible. We routinely create a 1.5×1.5 cm chip of 9 membranes. This recipe is straightforwardly extendable for full wafer process.

2. Experimental

The silicon nitride SiN_x thin film is deposited in a dual chamber system. The PECVD chamber is used to deposit the dielectric film, while the ICP RIE chamber is used to pattern the etching window. These two chambers are separated by a load-lock that provides in-situ fabrication possibility.

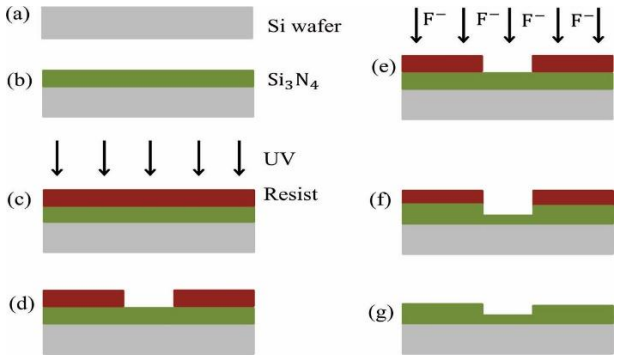

Figure 1. Recipe to pattern the SiN_x films with the dry etching process: (a) the native silicon dioxide layer on silicon wafer is removed using HF, (b) The Si_3N_4 layer is deposited by PECVD. (c) Spin coating photoresist and exposing photoresist to UV light with a photolithographic mask. (d) Developing in TMAH 2.5% to open the etching window. (e) Dry etching using reactive-ion etching in the ICP-RIE chamber. (f) The specimen after the dry etching process. (g) Photoresist removal and cleaning.

Prior to the deposition, a 275 µm thick silicon wafer is soaked in hydrofluoric acid for 30 seconds to remove the native oxide layer. It is then quickly transferred to the load-lock and pump down. It is important that the transfer step is fast, as native oxide grows quickly on the fresh Si surface. Even an ultrathin SiO_2 layer between Si and SiN_x could lead to over-etching in the KOH etching step and thus lift off the SiN_x layer subsequently. In the PECVD chamber, the radio frequency (RF) discharge creates a plasma environment that ionizes SiH_4 and NH_3 ion. The chemical reaction occurs as $Si^{4+} + N^{3+} \rightarrow Si_3N_4$. Calibration with temperature and pressure yields 317 ℃ and 0.3 Torr [20]. The best RF power is 7 W, although the power of 10 W also works nicely. Using a spectroscopic ellipsometer, we characterize SiN_x thin film optical properties as a function of FR_{NH_3}/FR_{SiH_4} , with FR_{NH_3} is the NH_3 flow rate and FR_{SiH_4} is the SiH_4 flow rate. The obtained band gap is used to determine the depositing condition of Si_3N_4 thin film. Typically, FR_{SiH_4} is fixed at 10 sccm while changing FR_{NH_3} from 20 sccm to 80 sccm. To reach a higher FR_{NH_3}/FR_{SiH_4} value, we continuously change the flow rate of SiH_4 from 9 sccm to 5 sccm while fixing FR_{NH_3} at 80 sccm. Similarly, SiH_4 and N_2O are used to fabricate silicon dioxide thin film in the PECVD chamber. The SiO_2 thin film is deposited at temperature of 317 ℃, pressure of 0.4 Torr and FR_{N_2O}/FR_{SiH_4} = 80 sccm/ 4 sccm.

After the deposition in the PECVD, etching windows are patterned on the Si chip using standard optical lithography. The resist AZ 5214E is spun at 4000 rpm for 1 minute, followed by 1 minute bake at 110 ℃. The resist is exposed for 5 s at 10 mW/cm^2 power density. It is developed in tetramethylammonium (TMAH) 2.5 % for 30 s. The chip with patterned resist is then loaded into the RIE chamber, and reactive ion etched with SF_6. Here, the gas flow is 50 sccm, the pressure is 0.03 Torr, capacitively coupled plasma power is 20 W, and inductively coupled plasma power is 200 W. To obtain the dry etching rate, we use a profilometer to measure the depths of "SiN_x wells" as a function of the etching time.

The Si_3N_4 Suspended Membrane

We use a solution of 20% KOH to etch Si at 80 ℃, which results in an etching rate of 1.8 µm/min [21]. To ensure anisotropy etching, 10% isopropyl alcohol IPA is added to the solution. Typically, it takes more than 5 hours to etch through the 275 µm thick wafer. In this paper, the etching apparatus is set up for a single chip of 1.5 x 1.5 cm^2. A full wafer etching system is under construction.

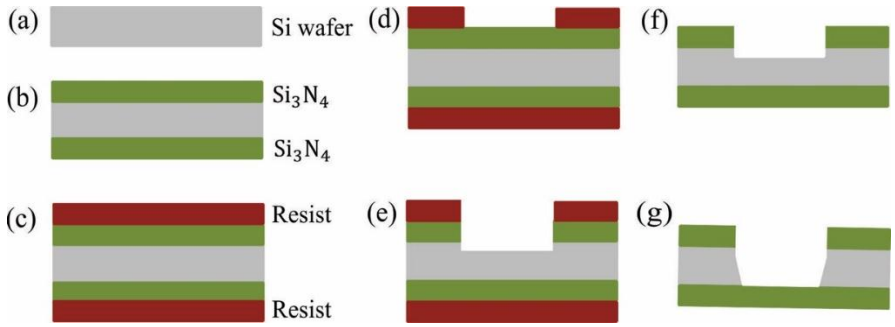

Figure 2. Fabrication process for Si_3N_4 membranes: (a) cleaned silicon wafer. (b) Depositing Si_3N_4 on both side of the chip. (c) Spin coating photoresist on both sides of the wafer. (d) Opening the etching window on the backside of the wafer using photolithography. (e) Dry etching Si_3N_4 in SF_6 plasma. (f) Removing photoresist using acetone. (g) Wet etching in KOH solution.

The recipe to fabricate the suspended Si_3N_4 wafer can be summarized as the diagram in Figure 2: first, the silicon wafer is diced into 1.5×1.5 cm chips, and dip in HF for 30 s. Si_3N_4 thin films are deposited on both sides with identical parameters. Because KOH etches photoresist, the back-side Si_3N_4 acts as a mask during this etching step. Photolithography patterns the backside of the chip with circles of 600 µm diameter. We then use reactive ion etching to open the SiN_x windows from the backside. The chip is wet etched in KOH through this etching window until it is stopped by the top SiN_x layer.

Optical properties of the SiN_x thin films are measured using a spectroscopic ellipsometer. This measurement indirectly measures through the ellipsometric angles. It is necessary to create a model for our sample to deduce the sample parameter like thickness and optical constant. We used amorphous model to fit our SiN_x. Here, the refractive index n and the extinction coefficient k of the material are described by these following equations:

$$n(E) = \frac{B_0.E + C_0}{E^2 - B.E + C} \quad \text{and} \quad k(E) = \begin{cases} \frac{A(E - E_g)^2}{E^2 - B.E + C} & E > E_g \\ 0 & E \leq E_g \end{cases}$$

Where:

$$B_0 = \frac{A}{Q}\left(-\frac{B^2}{2} + E_g.B - E_g^2 + C\right)$$

$$C_0 = \frac{A}{B}\left[(E_g^2 + C).\frac{B}{2} - 2.E_g.C\right]$$

$$Q = \frac{1}{2}.\sqrt{4C - B^2}$$

Here, B_0, C_0, and Q are obtained from fitting parameters A, B, C. E_g is the band gap energy, A is a parameter depending on the dipole matrix squared and describe the strength of the extinction coefficient peak. $B = 2E_0$ and $C = E_0^2 + \Gamma_0^2$ are expressions of physical parameters. The experiment data must be fitted with the model of the sample before deducing the sample parameters [22]. This model allows us to calculate the band gap E_g of the SiN_x thin films. We optimize the fabrication conditions for Si_3N_4 thin film based on this value.

3. Results and Discussion

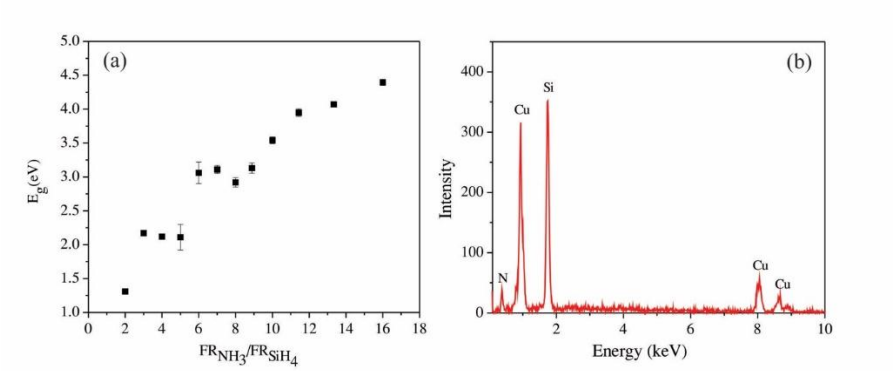

Figure 3. (a) The band gap of SiN_x deposited at different FR_{NH_3}/FR_{SiH_4} measured using spectroscopic ellipsometry. Si_3N_4 is obtained at FR_{NH_3}/FR_{SiH_4}=16. (b) Energy dispersive x-ray spectrum (EDS) of the sample showing Si and N component. Cu peaks are an artifact from the copper tape used to immobilized the sample.

It is important to deposit SiN_x with the correct ratio such that the stoichiometry is Si_3N_4, the most thermodynamically stable form. Our thin film's band gap and its optical properties are obtained from fitting experimental ellipsometry spectra with models using the above-mentioned amorphous dispersion relation for the active layer. Figure 3 shows the dependence of the SiN_x band gap on the flow rate ratio FR_{NH_3}/FR_{SiH_4}. The data with flow rate ratio from 0 to 9 is taken such that the flow rate of NH_3 is kept constant at 80 sccm while the flow rate of SiH_3 is changed from 10 sccm to 5 sccm. For flow rate ratio from 9 to 18, the flow rate of SiH_4 is kept at 10 sccm, and the flow rate of NH_3 is changed from 20 to 80 sccm. It is clear that the increase of FR_{NH_3}/FR_{SiH_4} resulted in an increase of band gap of SiN_x. From this result, SiN_x deposited with FR_{NH_3}/FR_{SiH_4}= 80 sccm/ 5 sccm has band gap of 4.394 eV, the closest to the band gap of Si_3N_4 [23]. This result is reconfirmed with an energy dispersive X-ray spectroscopy measurement EDS (data not shown).

The etching rate of Si_3N_4 using ICP RIE is an important parameter. Figure 4 shows the dependence of the depth of the wells as measured from the profilometer on RIE etching time. The SF_6 plasma first etches the Si_3N_4 film. Upon completion, Si etching continues. These rates of the two processes are corresponding to two slopes in Figure 4. The etching rate of SiN_x is 0.8 nm/s and the etching rate of Si is 9 nm/s with 50 sccm SF_6 gas, 0.3 Torr pressure, capacitive coupled plasma power of 20 W, and inductive coupled plasma power of 200 W.

With a proper Si_3N_4 thin film and a correct etching rate, we fabricate the suspended Si_3N_4 membrane. Figure 5 shows optical images for some of our Si_3N_4 membranes. Miller indices create the plane in a silicon crystal as {100} correspond to the front view, {110} to edge view, {111} to vertex view. In the wet etching with KOH corrode silicon in {100} direction much faster than {111} direction as in the diagram shown in figure 5 (a). Wet etching in KOH is well-executed that selective rate at different crystal orientation is clearly demonstrated. The tilt angle as seen from the back side in Figure 5c is an exact 54.7 degree, agree with previous literature [24]. Furthermore, a circular photolithographic mask results in an octagonal shape in Figure 5b.

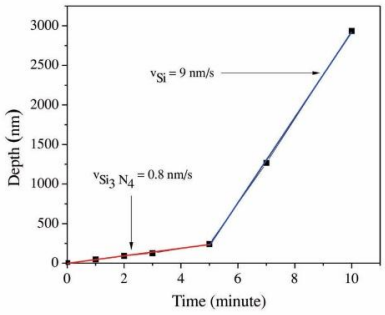

Figure 4. The dependence of the Si_3N_4 well depth on RIE etching time. The Si wafer is etched at a much faster rate upon the completion of the Si_3N_4 layer. Here, the plasma power is 20 W at pressure 0.03 Torr and the SF_6 gas flow is 50 sccm.

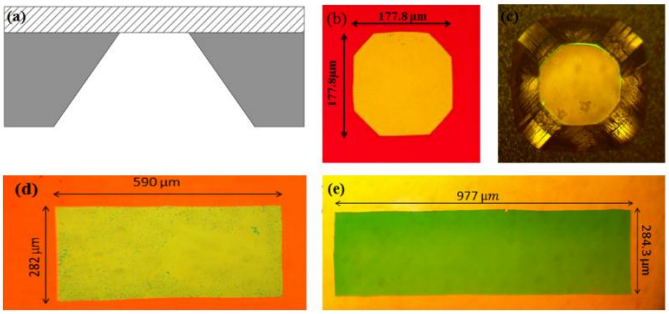

Figure 5. (a) Cross section diagram of the suspended Si_3N_4 membranes. The thickness of Si_3N_4 is 100 nm, while Si wafer is 275 µm, (b) Top view of the Si_3N_4 membrane prepared with round photolithography mask, (c) Bottom view of Si_3N_4 membranes after wet etching by KOH 20% solution, (d) and (e) ultra large membrane of different rectangle sizes.

In this work, we produce membranes of three sizes: 1000 µm × 300 µm, 600 µm × 300 µm and 200 µm × 200 µm. To account for the etching angle, the photographic mask dimensions are 1400 µm × 700 µm, 1000 µm × 700 µm, 600 µm × 600 µm, respectively. The yield is listed in Table 1. Apparently, the larger the windows size, the lower the yield. It is worthwhile to note that a window's size of 1 mm is a macroscopic scale that only required in special applications. To have a higher yield, it is better to fabricate membranes with a size less than 100 µm.

The silicon nitride membranes have an atomically flat surface as shown by the scanning electron micrograph and atomic force micrograph in figure 6. Clearly, Si_3N_4 thin films are not corroded by OH^- ion during the wet etching process. The membrane is compatible with other nano fabrication process. Together with the low thermal conductivity and mechanical durability, it is an ideal platform for a wide range of applications.

Table 1. A list of membranes fabricated in this work. The Si substrate is 275 µm thick. The Si_3N_4 membrane is 100 nm thick.

Shape	Dimension	Figure	Number of membrane made	Yield
Octagonal	177.8 µm × 177.8 µm	5b	14	51.9 %
Rectangle	282 µm × 590 µm	5d	3	50 %
Rectangle	284.3 µm × 977 µm	5e	1	16.7 %

We have employed this membrane for two research directions in our group. In one application, we deposit conducting wire on the membrane and measure thermal conductivity using 3ω method [25]. Once the value for Si_3N_4 is known, we can determine the thermal conductivity of any thin film deposited on top [26]. Thus, it is a universal platform to measure thin film thermal conductivity. In another application, we fabricate thermoelectric cooler using Peltier effect in BiTe and SbTe [27], the most popular pair of the thermoelectric material. The hot part of the cooler is placed on the bulk Si wafer, while the cold metallic part is placed on the membrane. Due to low thermal conductivity, the cold part is isolated from the environment, and thus ensure the superiority of this cooler. This cooler is compatible with nano-fabrication and could control temperature locally at the micron scale.

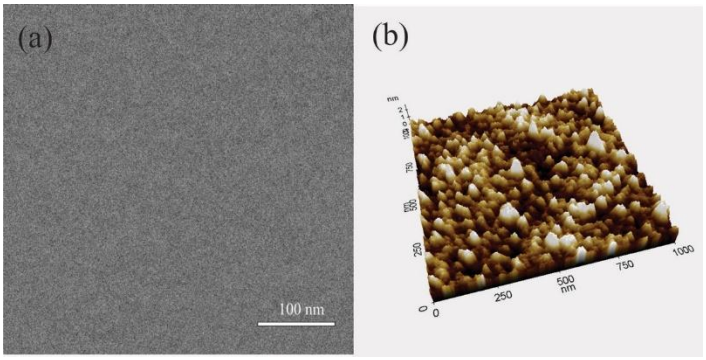

Figure 6. (a) Scanning electron micrograph and (b) atomic force micrograph of the suspended membrane showing an atomic flat surface. The thickness scale on the AFM image is on the order of 1 nm.

4. Conclusions

Using plasma enhanced chemical vapor deposition and wet etching method, we successfully fabricated ultra-thin Si_3N_4 suspends membranes of various size and shape. Si_3N_4 thin films were deposited on silicon wafer with FR_{NH_3}/FR_{SiH_4} = 80 sccm/ 5sccm at 317 ℃ at 7 W power. The etch rate of SiN_x and Si are 0.8 nm/s and 9 nm/s, respectively with the following dry etching condition: 50 sccm SF_6 gas, 0.03 Torr pressure, CCP of 20 W, and ICP of 200W. For 275 μm thick Si wafer, the etching time in KOH is about 5 hours. We successfully fabricated the Si_3N_4 membranes with different sizes, and the biggest size is 1000 μm × 300 μm. The capability to self-support the suspended membrane has open new research direction for us, especially in power-MEMS.

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