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Original Article

Void-Defect Location Control of Laser-Crystallized Silicon Thin Films with Hole-Pattern

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Abstract: High-performance low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have been developed for larger applications than flat panel displays (FPDs) such as three-dimensional integrated circuits (3D-ICs) and glass sheet computers. The crystallinity of poly-Si thin films has been the key factor determining TFTs' performance. In this work, a void-defect location has been controlled by patterning amorphous silicon (a-Si) thin films with rectangular and square holes before crystallized by multiline continuous-wave laser beam to avoid the effect of void-defects on the TFTs' performance. Instead of randomly appearing in the poly-Si thin films, void-defects were only observed at the backsides of the patterned holes. Interestingly, large crystal grains without void-defects were laterally crystallized at Si strips between holes. By observing the crystallinities of poly-Si thin film around the patterned holes, both the mechanism of the void formation and crystal growth based on temperature gradient was clarified.

Keywords: Poly-Si thin film, Continuous-wave laser lateral crystallization (CLC), LTPS-TFTs.

1. Introduction

Uniformity of high-performance low temperature polycrystalline silicon (Poly-Si) thin-film transistors (TFTs) has been the key target for commercialization in the flat panel display (FPD)

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market, three-dimensional integrated circuits (3DICs) [1-3]. Uniform LTPS-TFTs have been obtained with excimer laser annealing (ELA) technology and successfully applied in the FPD for decades. However they have a low mobility, below 200 $cm^2V^{-1}s^{-1}$ with small silicon crystal grains of 0.5-1 µm [4]. Other laser-crystallization methods such as sequential lateral solidification (SLS), solid-phase crystallization (SPC), thermal plasma jet (TPJ), and flash lamp annealing (FLA) have been applied to grow large crystal grains, and high-performance LTPS-TFTs have been achieved [5-7]. However, the uniformity of TFT's performance has not been achieved by these methods since the non-uniform crystallinity of poly-Si thin films have been formed. Continuous-wave laser lateral crystallization (CLC) has been developed to get large crystalline grains, hence the high-performance LTPS-TFTs have been achieved [8]. However, it has been found that the poly-Si thin films have a random crystal orientation and LTPS-TFTs have a high variation in their performances. The crystal orientation of poly-Si thin films was not uniform because of Gaussian distributed laser beams. This disadvantage has been improved by applying laser optics including a diffractive homogenizer, expander, and shrinkage lens, the Gaussian laser beam was deformed into a multi-line beam (MLB). As Kuroki et al. reported in [9], uniformly (211)-(110)-(111) poly-Si thin films have been crystallized at high laser exposure energy conditions utilizing the MLB-CLC [9]. Moreover, highly (100)-surface-oriented poly-Si thin films have been achieved at a low laser exposure energy regime with overlapped scans, and then ultrahigh-performance LTPS-TFTs with ultrahigh-electron field-effect mobility up to 1010 $cm^2V^{-1}s^{-1}$ have been realized [10-12]. However, uniformity has not been attained due to both the variation of crystallinity and the number of voids in the poly-Si films. These voids significantly affected the uniformity of TFTs' performance as they were located at the TFTs' channels.

In this work, we reported the effect of voids on the TFTs characteristics. Moreover, to prevent the formation of voids at the channels, we controlled the location of voids by patterning the a-Si thin films with square and rectangular holes before irradiating them. In addition, the formation mechanism of the voids has also been discussed.

2. Experimental

Laser-crystallized poly-Si thin films were prepared as follows: (1) A SiO_2 buffer layer of 1 µm was deposited on a quartz substrate by plasma-enhanced chemical vapor deposition (PECVD); (2) An amorphous silicon (a-Si) thin film of 150 nm was deposited on the SiO_2 layer buffer layer by PECVD; (3) The a-Si film was then covered by a 100 nm SiO_2 cap layer by PECVD; (4) These samples were annealed at 490 °C in N_2 ambient for dehydrogenation for an hour, and (5) The samples were irradiated by a diode-pumped solid-state continuous-wave laser of 532 nm wavelength by the MLB-CLC for non-patterned poly-Si thin films. For hole-patterned poly-Si thin films, after the samples were prepared as steps (1) - (4), the cap SiO_2 and a-Si films were patterned with square or rectangle holes by photolithography, followed by wet etching. The cap SiO_2 holes were etched by buffer hydrofluoric acid (BHF) and the a-Si film holes were etched by tetramethylammonium hydroxide (TMAH) at 70 °C. Finally, these samples were irradiated by a multiline beam continuous-wave laser of 532 nm wavelength at the same laser crystallization conditions.

Figure 1a shows the top-view profile of the laser beam. It is seen that the laser density is distributed in multiline beams. The laser crystallization was carried out at 6 W laser power and 0.8 cm/s scanning speed, and 200 µm width of overlapped scan region. The schematic of an a-Si sample and its laser scanning process is shown in Fig. 1b. Figure 1c shows the schematic of a hole-patterned sample and its irradiation process. The holes were designed with various diameters from 10 to 20 µm

sides and located in lines that were perpendicular to the scanning direction. The Si strips were created between patterned holes. Their width also varied from 10 to 20 μm.

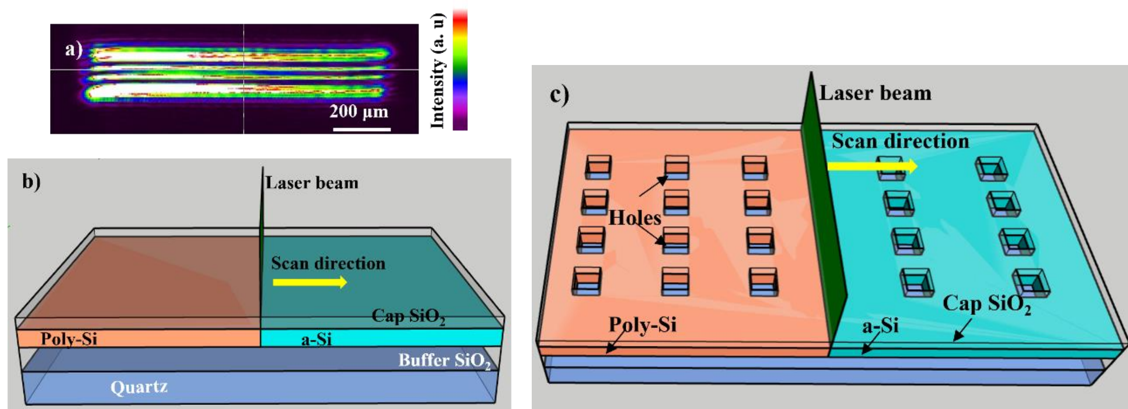

Figure 1. The top-view profile of MLB-CLC (a), the laser scanning process schematic of non-patterned (b) and hole-patterned Si thin films (c).

LTPS-TFTs were fabricated in an ISO 4 clean room as follows: After the cap SiO_2 layer was etched by buffered hydrofluoric acid (BHF) solution, the poly-Si active regions were patterned using photolithography and dry etching. 42 nm SiO_2 insulator was deposited by Electron Cyclotron Resonance (ECR) Plasma Chemical Vapor Deposition at 300 °C, and a 300 nm - thick Mo layers were deposited by sputtering. Patterning of the gate electrodes was carried out by lithography and wet etching followed by self-aligned source and drain formation by As ion implantation (ion dose: 2×10^{15} cm^{-2}, accelerating voltage: 66 kV), using the Mo gate as a mask. Activation annealing treatment was performed at 550 °C in N_2 ambient for 30 minutes. Before SiO_2 interlayer dielectric film of 600 nm thickness was deposited by Atmospheric Pressure Chemical Vapor Deposition (APCVD), sacrificial SiO_2 in the source and drain region was etched by BHF. The contact holes were formed by lithography and BHF wet etching. 700 nm - thick Mo pads were deposited by sputtering and patterned by lithography and wet etching. Finally, the sample was annealed at 400 °C in H_2 ambient for 30 minutes.

The surface morphology and crystallinity of laser-crystallized poly-Si thin films were observed by microphotograph, scanning electron microscope (SEM). The crystallinity of the poly-Si thin films was observed by electron back-scattering diffraction (EBSD).

3. Results and Discussions

Figure 2 shows a microphotograph and SEM image of a non-patterned poly-Si thin film formed by MLB-CLC. The crystallization was carried out at 6 W laser power, 0.8 cm/s scanning speed, and 200 overlapped width. It was found that a considerable number of voids casually appeared in the film (Figure 2a). A void observed by a high-current SEM is shown in the image located at the upper-right corner of Fig. 2b. It appeared as a deep empty hole and occupied a large area of approximately 1 μm in the film. The density of the voids was averaged at about 0.21 voids in 10×10 μm^2 area. In addition, the voids heavily appeared in lines along the scanning direction. The distance between heavy-void lines was dependent on the overlapped width of irradiated regions.

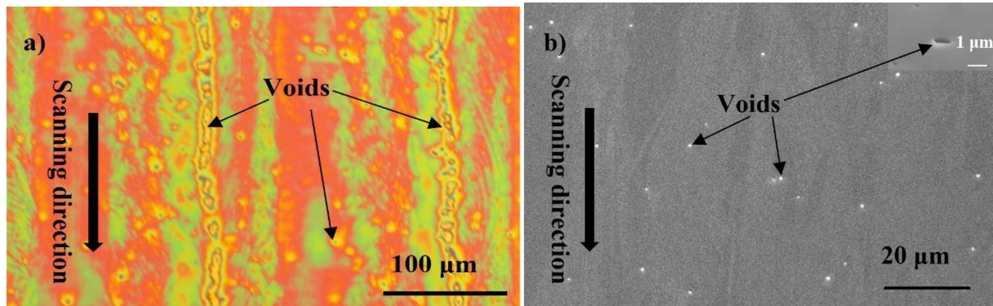

Figure 2. Microphotograph (a) and SEM images of the non-patterned poly-Si thin film formed by MLB-CLC (b).

Figure 3a shows the electrical characteristics of a typical TFT fabricated at a heavy-void region of non-prepatterned poly-Si thin film. The TFT's channel width and length are of 10 µm. Obtained result shows that the TFT has maximum electron field effect mobility of 91 $cm^2V^{-1}s^{-1}$, a threshold voltage of -0.7 V, a sub-threshold slope of 500 mV/dec, and ON/OFF ratio of 10^2. These performance values were much lower than those of TFTs reported in [10]. Figure 3b shows grain mapping of the poly-Si channel of the above-fabricated TFT observed by EBSD. It indicates that the poly-Si channel has close to (100) surface orientation. The channel has a width of ~ 3 µm, much narrower than the designed value (namely 10 µm). This is due to voids gathering in the channel. Therefore, the TFT's ON current decreased. The voids significantly induced a high variation in TFTs' performance.

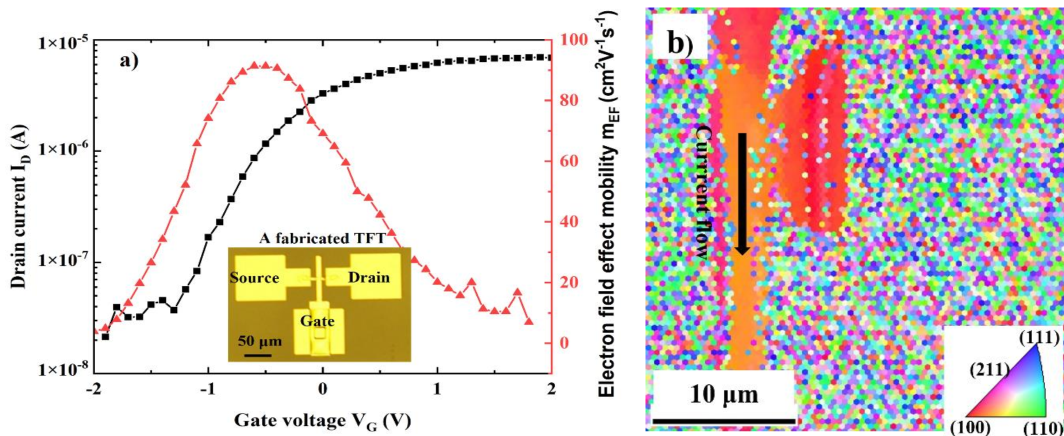

Figure 3. Electrical characteristics of a typical fabricated TFT (a)
and grain mapping of poly-Si TFT's channel measured by EBSD (b).

To control void location in the poly-Si thin films, rectangular and square holes were patterned with various sizes before crystallization. Figure 4 shows the microphotographs and SEM images of the rectangular and square hole-patterned poly-Si thin films. The sizes of rectangular holes and square holes were 10×20 μm^2 and 10×10 μm^2, respectively. The Si strips made between holes had 10 µm width. The laser exposure energy conditions of these poly-Si thin films were different to attain lateral crystallization at the Si strips. The laser power was fixed at 6 W. The scanning speed was carried out at 0.5 cm/s and 0.8 cm/s for the rectangular and square hole-patterned poly-Si thin films, respectively.

It is found that the void disappeared at the Si strips between holes and the front of holes and Si trips, although they are randomly formed in other regions for rectangular hole patterned poly-Si thin film, or they appeared at the back of the holes for the square one. This result indicates that the voids were controlled out of the Si strips that would be designed as TFTs' channels.

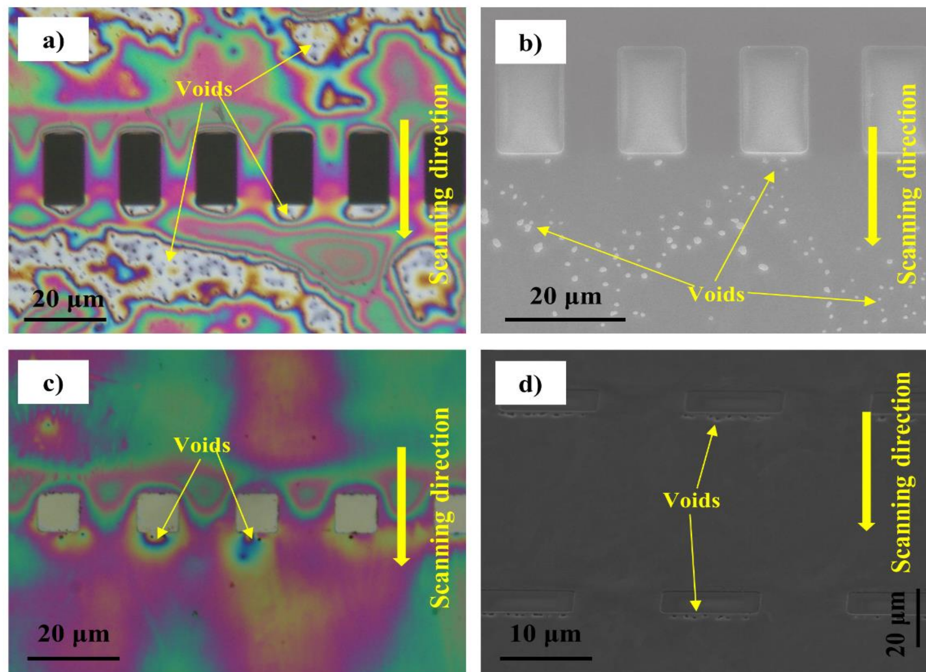

Figure 4. Microphotograph (a) & SEM image of rectangular hole patterned poly-Si thin film (b), Microphotograph (c) & SEM image of square hole patterned poly-Si thin film (d).

Crystallinities of the hole-patterned poly-Si thin films were measured by EBSD. Figures 5a, 5b, and 5c show grain mappings of the square hole patterned poly-Si film measured by EBSD at a random Si strip in the surface, scanning, and transverse directions, respectively. Their color maps corresponding to crystal orientations and rotation angles of grain boundaries are shown in Fig. 5d. It is seen that the Si thin film was completely lateral-crystallized. The large crystal grains typically grew along the scanning direction that is the longitude direction of Si strips and there was no void at the Si trip. The crystal grains around the Si strips were large and had typically (100) surface orientation. Their crystal orientations in the scanning and transverse directions were between (100) and (110) planes. Small angle grain boundaries of below 10° were typically observed in this film. This poly-Si thin film is promising to achieve a uniformity of ultrahigh-performance LTPS-TFTs owing to typical (100) surface-oriented Si crystals with no void and few grain boundaries appearing at the predefined TFTs' channels.

Si crystal growth is based on the temperature gradient in the liquid Si region, and void-defect formation is caused by crystal grains non-laterally growing [13]. It is noticed here that the lateral crystallization can be achieved only if the laser exposure energy is in a suitable range [9]. In the non-patterned poly-Si thin film, the temperature gradient pointed to the scanning direction. The appearance of voids was caused by some random nucleations among liquid Si due to its temperature varied at the Si melting point. Hence, some voids were randomly formed between crystal grains growing in different directions. In the hole-patterned poly-Si thin film, the temperature of liquid Si films around

the air holes decreased due to a lower laser absorption. The exposure energy of the 10×20 μm^2 rectangle-hole patterned poly-Si film was larger than that of the 10×10 μm^2 square hole patterned film. To obtain lateral crystallization at the rectangular Si strips shown in Figures 4a and 4b, a non-patterned a-Si area was exposed with high energy, and the lateral crystallization was destroyed.

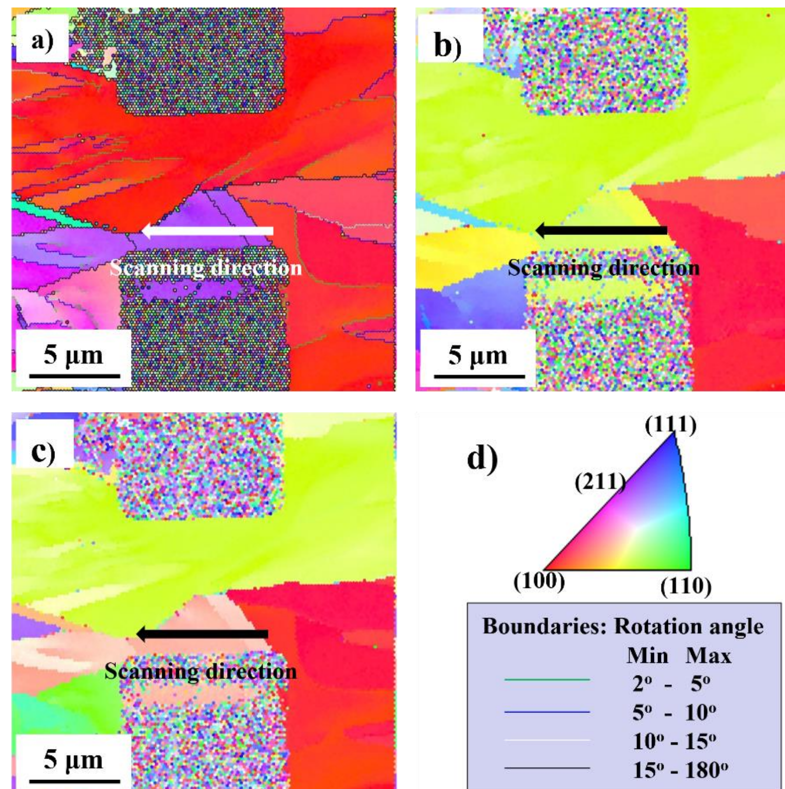

Figure 5. Grain mappings of square hole poly-Si thin film measured by EBSD in a) surface, b) scanning, c) transverse directions, and d) their color maps.

In the hole-patterned poly-Si thin film shown in Fig.s 4c and 4d, the lateral crystallization was achieved at square Si strips and other regions. Moreover, the heat flow at the interface between liquid Si strips and the air was negligible and the temperature was stable there. The voids therefore disappeared at the Si strips thank to the lateral growth of crystal grains. Contrastingly, the lowest temperature regions were at the backsides of the holes and the temperature gradient was divergent there. Nuclei started being randomly formed at these sides and their crystal growth directions were divergent. Void-defects were observed in these regions.

4. Conclusion

To control void-defect location, rectangular and square hole patterns were applied to a-Si thin films before irradiated by the MLB-CLC. Instead of randomly appearing in the poly-Si thin films, void-defect location was controllable in the hole patterned poly-Si thin films. Voids were only observed at the backsides of the patterned holes but did not appear at the pre-defined Si strips between

holes. The crystallinities of the poly-Si strips were very good with large crystal grain growing along the strips. The effect of void-defects formed into the laser-crystallized poly-Si thin film on LTPS-TFTs' performance was reported. Therefore, large crystal grains without voids designed for TFTs' channels can significantly improve TFTs' performance and uniformity.

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