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Original Article

# Design and Implementation of an S-band Receiver for Small Satellite Based on the Manufactured Subsystems

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**Abstract:** In this work the design and implementaion of a receiver for small satellites in range of 1.9 GHz to 3.0 GHz frequency were presented. We concentrated on developing a new architecture for receiving satellites in challenging environments and integrated some of the author's previously published designs. By using the protected mechanism for RF circuit of receiver, a mutil-stage in IF amplifier and automatic gain control in IF amplifer has been designed, this receiver has a higher gain (78 dB), a larger dynamic ranger (80 dB), a high stability and sensitivity (110 dBm) at 2.15 GHz frequency. The receiver module works well; and due to the flexible structure, easy assembly and low-cost characteristics, it can be applied for small satellites and ground stations.

*Keywords:* LNA, mixer, S-band, receiver, IF amplifier.

## 1. Introduction

In recent years, space technologies have become increasly impotant for developping economy – society and security of a country. They are used in weather forecast, global positioning systems, maps, education, science, communication, etc. Satellite technique is a part of the space technology. Normally, a satellite has seven important subsystems, such as structure, thermal, payload, attitude determination and control, communication, electrical power and command & data handling.

A communication subsystem provides link between satellite and ground station. It transmits telementry data, payload data from satellite to ground station; tele-command data from ground to satellite. The communication subsystem consists of transmitter and receiver.

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Previous paper, authors has published a “the transmitter of Nanosatellite with new configuration” articles. By combining heterostructure field effect transistors (HFET) and laterally diffused metal–oxide–semiconductor (LDMOS) technology and using flexible structure and flexible control method, this research obtained 60 dB gain power when input is -14 dBm, output power is 46 dBm (more than 25 W) in 2,1 GHz -2,3 Ghz frequency; phase noise is -80 dBc/Hz at 100 KHz offset frequency [1]. In this paper, authors present a receiver of small satellite, which was compatible with transmitter in [1].

Each receiver has different characteristic features dependent on user’s purpose. It must respond to requirements of the satellite system, such as noise figure, bandwidth, dynamic range, sensitivity, gain, stability. Designer of the receiver need to understand the tradeoff between accuracy, bandwidth and received power in the receiver, as well asto balance the targets. Comperingto the previous receiver, the protection problem of RF circuit was interested in the design. Some designers of the low noise amplifier (LNA) have used complementary metal-oxide-semiconductor (CMOS) technology and Electro Static Discharge (ESD) circuit to protect against high input power. As reported in [2], the ESD protection structure and LNA circuit were designed and implemented in 0,18 $\mu m$ SiGe BiCMOS technology. However, this ESD protection structure affects the performance of radio frequency integrated circuit (RFICs) [2]. Lin et al., [3] resolved this problem by stacking diodes with embedded silicon-controlled rectifier (SDeSCR) and SCR-based power clamp to protect the LNA. This structure is fabricated in CMOS technology.

Shabana has designed a satellite RF receiver at Ku-band for tropical region [4] with describing a basic component of receiver. However, the obtained result (namely LNA with 8.9 dB gain, bandwidth of 86 MHz) is not expectative.

Solution to low gain and narrow bandwidth is integrated in multi-stage. This novel design is a new configuration in a module. There are protection RF circuit, multi-stage and automatic gain control. This integrate module makes the receiver become better. There are highly sensitive, high power output, stability operation, and larger dynamic range).

This receiver consists of a LNA, followed by Mixer + LO, IF Amplifier was integrated AGC. This module is showed in Figure 1.

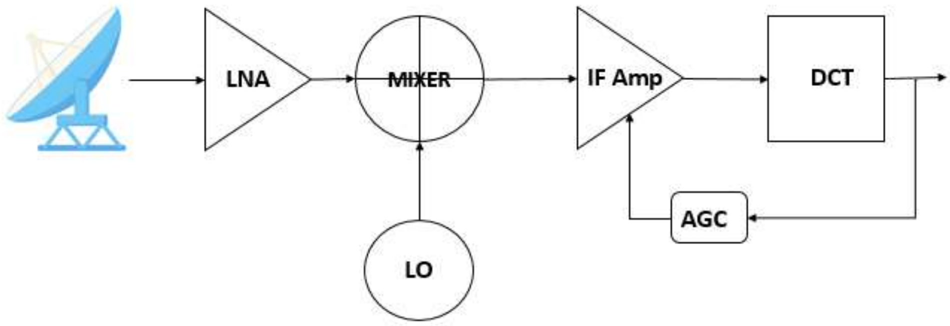


Figure 1. Block diagram of receiver module.

In this work we present a new configuration of a reciever. There are LNA with protection mechanism and multi-stage, down conversion with PLL phase lock loop and intermediate frequency (IF) amplifier with automactic gain control (AGC).

## 2. Design and Simulation

### *2.1. Low Noise Amplifier (LNA)*

A signal is received through antenna, going to Low Noise Amplifier (LNA). Here, signal is still weak, so a signal amplitude is amplified. LNA operates well when it responds system’s requirement. A good LNA is that has high gain and low noise figure. When deigning circuits, one need to a have good impedance matching, good electronic components. Special PCB layout is very important.

Besides, the protection of RF circuit is nesecsary. Some methods were used in published works, f.i. “Compact ESD protection Design for CMOS Low-Noise Amplifier”. The traditional Electro Static Discharge (ESD) protection circuit, dual diodes (DD) with MOS-based power clamp is a traditional onchip ESD. This method has disadvantages of large parasitic capacitance, large turn-on resistance, large layout area and large leakage current. To overcome these disadvantages, the “Compact ESD protection Design for CMOS Low-Noise Amplifier” used stacked diodes with embedded silicon-controlled rectifier (SdeSCR) and SCR-based power clamp power to protect the LNA. Specially, this protection method does not affect RF sigmal. This method was applied in CMOS technology.

In this design, LNA used PHEMT SPF-2086 of Sirenza with characteristics: frequency operation at 0.1 – 6 GHz with pHEMT GaAs FET, protection mechanism with PIN diode.

Herein, impedance matching is with quarter-wave transformer, with $Z_{in} = Z_0$*(2.136 + j2.199); $Z_{out} = Z_0$*(0.438 + j1.099). The LNA was designed and simulated at ADS softwave. The schema is showed in Figure 2.

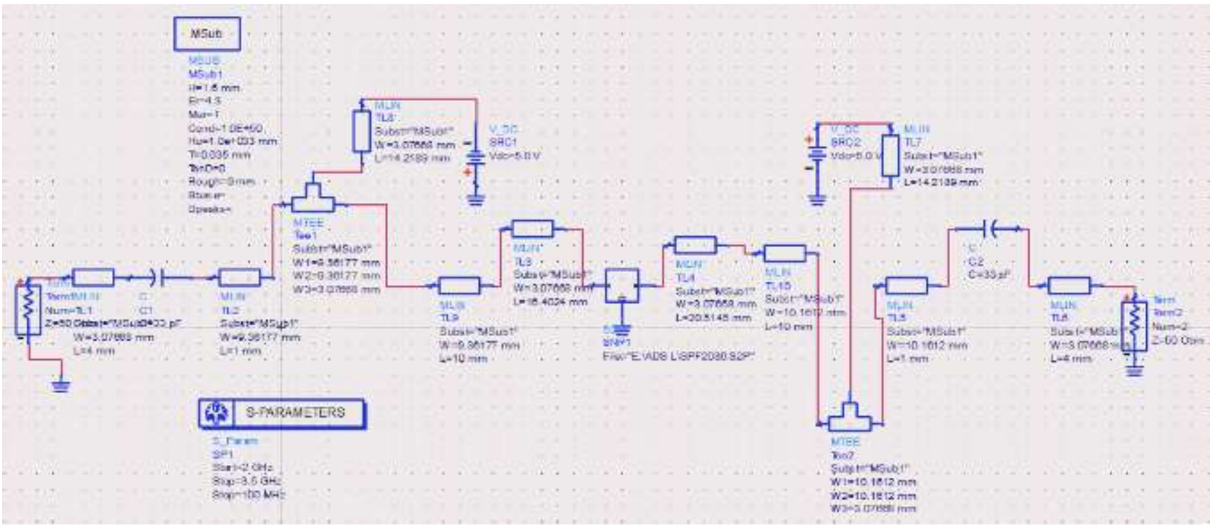


Figure 2. The schematic of LNA impedance matching.

The layout and manufactured LNA is showed in Figure 3 and Figure 4.

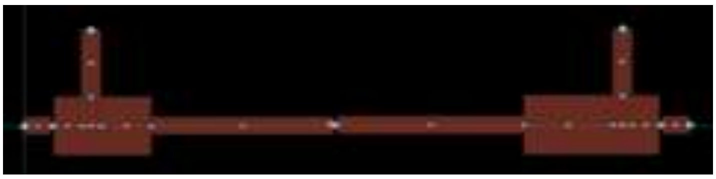

Figure 3. Layout of LNA circuit.

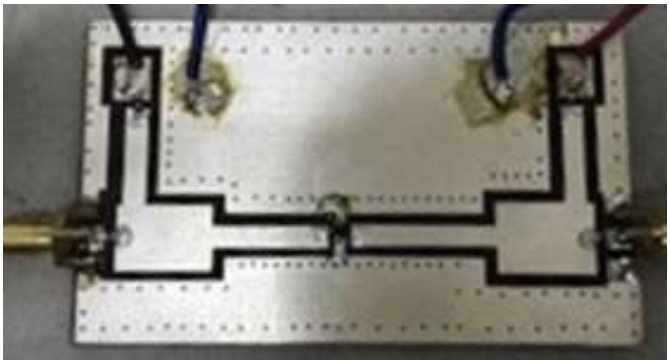

Figure 4. The fabricated LNA.

To optimazie LNA, two stages were integrated as shown in Figure 5.

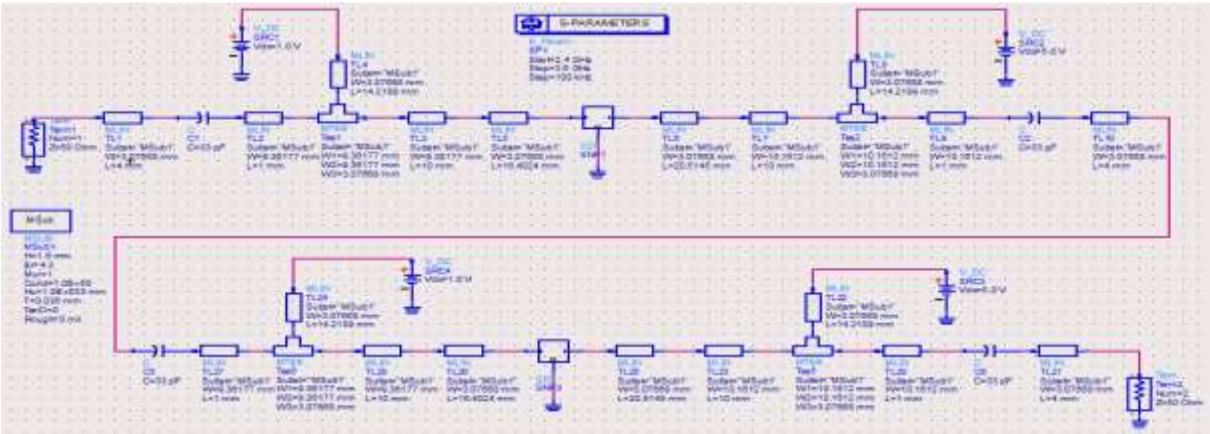


Figure 5. Schematic of 2-stages LNA.

## *2.2. Mixer*

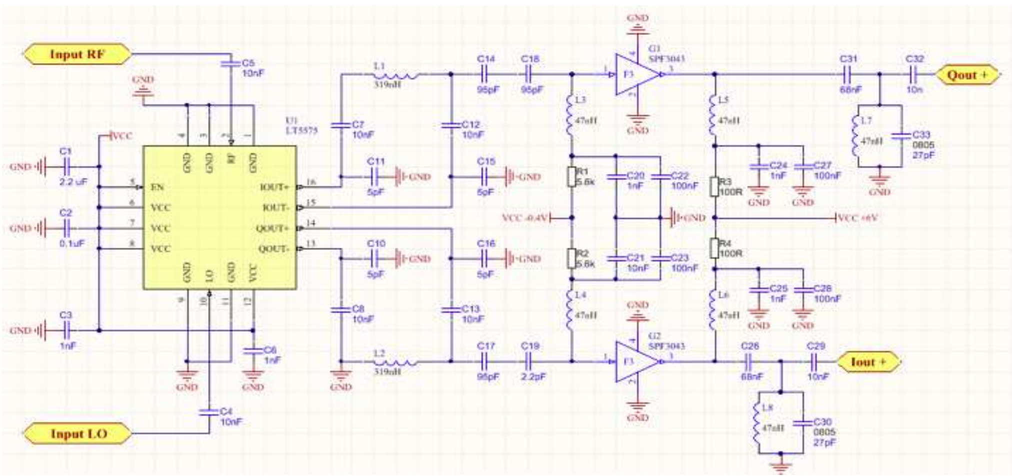


Figure 6. Schematic of mixer.

The mixer with output I/Q was designed and manufactured in 2019 as reported in [5]. By this module RF signals are converted to IF ones. The mixer used LT5575; The module generates local oscillator (LO) signals for mixer used phase lock loop (PLL) with ADF4113 and microcontroller AT89C51.

The schema of the mixer is illustrated in Figure 6. The module generating LO used phase lock loop (PLL) is showed in the Figure 7.

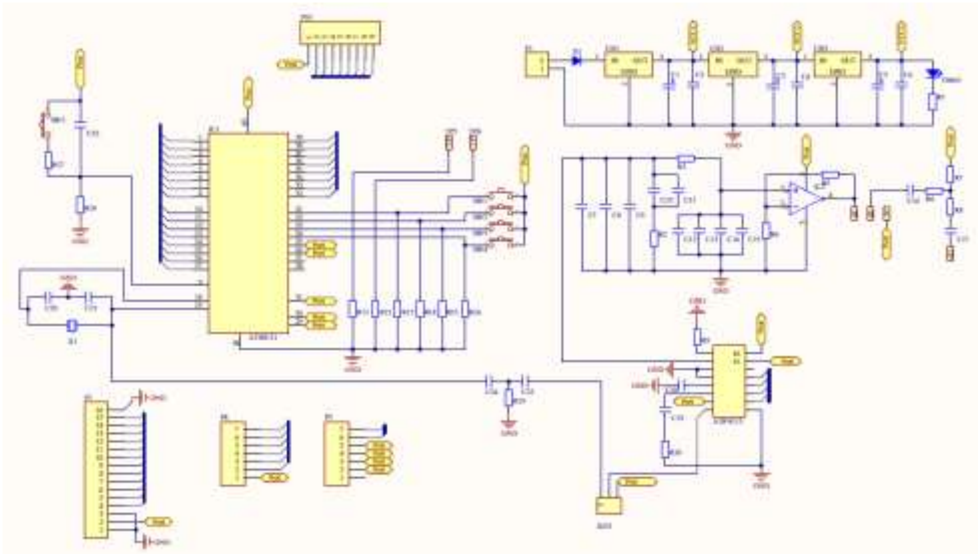

Figure 7. PLL with ADF4113 and microcontroller AT89C51.

*2.3. Intermediate Frequency Amplifier (IF Amplifier)*

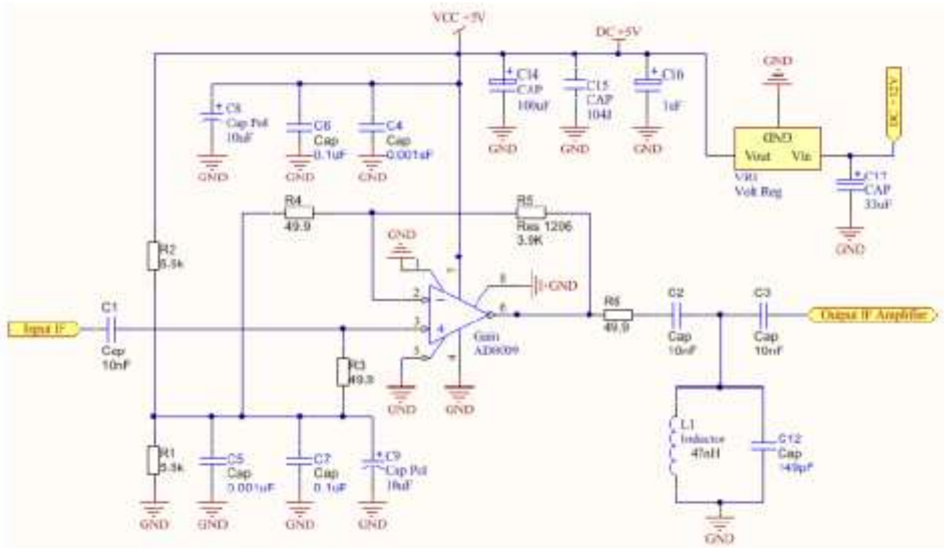


Figure 8. Schemetic of 1-stage IF amplifier.

IF amplifier is an important part of the receiver. It has main role in amplifier signal, dynamic range and bandwidth of the receiver. Multi-stage structure and amplifier gain control mechanism were combined in this design. The IF amplifier has three stages. Each stage was designed with different device/component. To obtain a largest gain power, it is neccessary to perform the impedance matching at output/input of each circuit.

This design consists of three-stages amplifier: the first stage with AD8009, the second-stage with AD8350, the third-stage with SPF3043. Figure 8 and Figure 9 show a part of the IF amplifier.

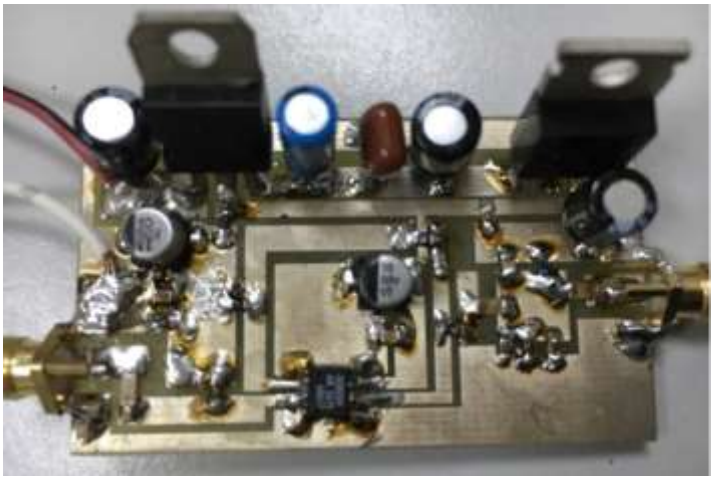

Figure 9. Board circuit of 1-stage IF amplifier.

## 3. Measurements Results

*Low Noise Amplifier (LNA)*

Figure 10. Set of measurement LNA.

Figure 11. Measurement result of LNA.

By using SPF 2086 for LNA circuit, the impedance matching in input/output is designed. This module (one stage LNA) gives 19.5 dB gain at 2.15 GHz . The noise figure is less than 1.5 dB. This LNA has a low noise figure, high gain.

*Mixer*

Figure 12. Set of measurement Mixer.

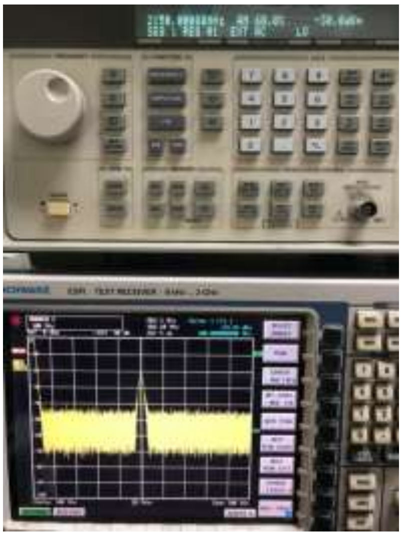

Figure 13. Measurement result of Mixer.

By using the down converter, RF signals 2.15 GHz are converted into intermediate frequency of 100 MHz. This module combined LO phase lock loop as above design, one can make desired IF frequency. The strength of the signal is not significantly reduced (input signal is -30 dBm, output signal is -23,1 dBm). It is also important factors for designing receiver of satellite.

*IF amplifier*

Figure 14. Set of measurement IF amplifier.

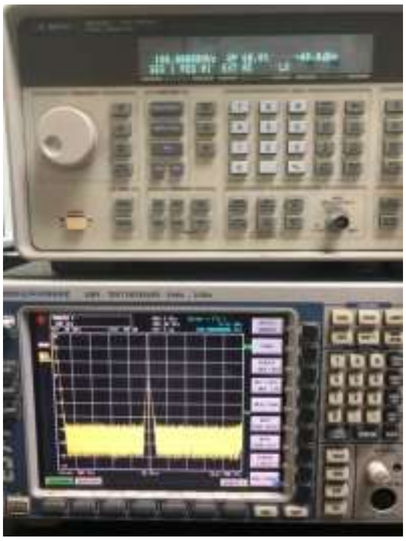

Figure 15. Measurement result of IF amplifier.

By the IF amplifier, one can increase the power of the signal for further processing. The amplified signal before going with input power of 40 dBm, output power is of 5.4 dBm. Losses in the cable/attenuator is 5 dBm. The measurement results proved that the designed module is a good IF amplifier.

*Integrated receiver module*

The receiver module is integrated and experimentally measured, as seen in Figure 16. This module havs I/Q channel output, large output power, low noise figure and high sensitivity. These parameters are illustrated in Table 1. At 2,15 GHz, IF frequency of 100 MHz, gain of 78 dB, sensitivity of 110 dBm and dynamic range of 80 dB were obtained.

Figure 16. Measurement of receiver module.

Table 1. The parameter of module receiver

| Parameter | |
|---|---|
| Frequency range, MHz | 1875 MHz – 3000 MHz |
| Bandwidth, MHz | 1125 MHz |
| IF frequency, MHz | 100 MHz |
| P_in, dBm | -70 dBm |
| P_out, dBm | 8 dBm |
| Gain, dB | 78 dB |
| Sensitivity, dBm | -110 dBm |
| Dynamic range, dB | 80 dB |

## 4. Conclusion

In summary, we presented the design and implementaion of a receiver for small satellites in range of 1.9 GHz to 3.0 GHz frequency. By using the protected mechanism for RF circuit of receiver, we have designed mutil-stage in IF amplifier and automatic gain control in IF amplifer, this receiver obtain a higher gain (78 dB), a larger dynamic ranger (80 dB), a high stability and sensitivity (110 dBm) at 2.15 GHz frequency. These results proved that this receiver module works stably and efficiently. In addition, this module has flexible structure, easy assembly, low cost characteristics. So, it can be applied for small satellites and ground stations.

## Acknowledgments

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