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Original Article

Design of a Compensation Network for an LLC Power Converter Applied to Motor Drive Control Systems under Rapid Load Variations

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Abstract: The paper focuses on the design of a Type II compensation network for a 500 W half-bridge LLC converter to stabilize a 60 VDC output voltage supplied to a motor under rapidly changing load conditions. By applying the K-factor method in combination with SIMPLIS-based simulation, the design parameters of the compensation network are selected and verified, enabling the system to achieve a crossover frequency in the range of 3.89 kHz - 4.6 kHz and a phase margin of 28.3°–37° across an input voltage range of 370-410 VDC. Experimental results show that when the load current changes abruptly from 0 A to 9 A, the output voltage undershoot is limited to 938 mV, while the overshoot during load removal is 705.5 mV. With the transient voltage deviation maintained below approximately 2% and the output voltage returning to steady state without sustained oscillation, the proposed compensation network improves the load-transient response and helps preserve the regulated DC output-voltage quality within the investigated operating range. These results support the feasibility of the compensated LLC converter for regulated drive-supply applications and provide a basis for further power-density improvement in future work.

Keywords: LLC resonant converter; Type II compensator; K-factor design; load transient response; BLDC motor drive; closed-loop control.

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1. Introduction

In modern DC–DC converters, the power stage is responsible not only for power conversion but also for providing galvanic isolation through a high-frequency transformer-based architecture [1]. Among the available approaches for increasing power density, increasing the switching frequency is regarded as one of the most effective solutions [2]. A higher switching frequency makes it possible to reduce the size and weight of passive components; however, this advantage is accompanied by an increase in switching losses and electromagnetic interference (EMI) [3, 4]. To address these challenges, resonant converters have been developed to enable semiconductor devices to operate under soft-switching conditions, including zero-voltage switching (ZVS) and zero-current switching (ZCS). In addition, the resonant current typically exhibits a nearly sinusoidal waveform, which contributes to lower switching losses and improved overall system efficiency [5-7]. Owing to these characteristics, resonant converters have emerged as a promising solution for high-power isolated power supply applications.

In specialized high-power applications, such as arc power supplies and industrial power systems, series resonant converter (SRC) and series–parallel resonant converter (SPRC) topologies have been shown to provide favorable operating performance [8, 9]. However, maintaining a stable output voltage under conditions of significant input voltage or load variations remains a major challenge, particularly for high-power DC–DC converters that require fast dynamic response. Consequently, the LLC topology has increasingly been adopted as an effective solution for providing a nearly constant output voltage, in combination with either diode rectification or synchronous rectification on the secondary side to improve system efficiency and transient performance [10, 11].

In brushless DC motor (BLDC) drive systems, the load frequently varies rapidly and discontinuously, requiring the power supply to exhibit minimal voltage sag and a fast voltage recovery capability. Several studies have focused on developing compensation strategies for LLC converters to improve output-voltage quality. Method [12] proposed an LLC converter with an output voltage of approximately 48 V. Method [13] presents a digital compensator for a 200 W converter, but did not report experimental results at the 60 V level. Meanwhile, method [14] employed resonant-frequency control with a reference voltage of 190 V. However, these studies have not comprehensively addressed the transient response of the converter under conditions of rapidly varying load current with large amplitude.

Against this background, this paper proposes a systematic design method for an analog Type II compensation network, based on the K-factor method, for a 500 W half-bridge LLC resonant converter. The objective of the study is to improve transient response and output-voltage stability under abrupt large-signal load variations from 0 A to 9 A. By tuning the closed-loop transfer-function parameters and validating the design through SIMPLIS-based simulation and prototype testing, the system achieves a regulated 60 VDC output with a transient voltage deviation maintained within approximately 2% under the investigated load-step conditions. These results contribute to regulated power supplies for BLDC motor-drive applications and wireless power transfer (WPT) downstream regulation stages, while also mitigating overshoot and undershoot during load connection and disconnection.

The novelty of this work is a quantified Type II analog-compensation design procedure and its experimental verification for a 500 W half-bridge LLC converter under a large-amplitude 0–9 A short-duration load-step condition. The work combines K-factor-based compensator design, SIMPLIS-based closed-loop verification, and prototype-level transient validation at a regulated 60 VDC output. This integrated design and verification procedure is particularly relevant for regulated 60 VDC supplies used in BLDC motor-drive systems and wireless-power-transfer downstream regulation stages, where the load can change rapidly, and the output voltage must recover without sustained oscillation. Therefore, the proposed circuit solution provides not only a compensation-network design but also an experimentally validated implementation for applications involving rapid load variations.

The remainder of this paper is organized as follows. Section 2 presents the LLC converter topology and the proposed compensation network. Section 3 describes the compensation design procedure. Section 4 analyzes the simulation and experimental results. Finally, Section 5 concludes the paper.

2. LLC Resonant Converter Topology and Compensation Network

2.1. Block Diagram of the Control System

Figure 1 illustrates the generalized block diagram of the LLC resonant converter under a feedback control scheme. The control loop can be represented by three principal blocks, including the power converter H(S), the feedback compensator G_c(S), and the switching-frequency modulation block. In this configuration, the LLC power stage serves as the core element governing the system's dynamic behavior, whereas the compensator and the frequency-modulation block are employed to shape the transient response and maintain output-voltage regulation.

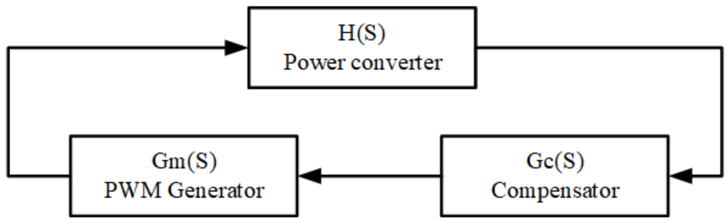


Figure 1. Block diagram of the LLC resonant-converter control system.

The G_m(S) block converts the control signal generated by the compensator into variations in the switching frequency, thereby enabling output-voltage regulation through the frequency-modulation mechanism inherent to the LLC converter.

2.2. Power Circuit Diagram and Operating Principle

Figure 2 illustrates the closed-loop circuit configuration of the half-bridge LLC resonant converter. In this topology, the power semiconductor switches are driven alternately with an approximately 50% duty cycle. A dead time is inserted between the turn-on and turn-off transitions to ensure safe operation of the semiconductor devices while also facilitating the soft-switching process.

The resonant tank of the converter consists of a resonant inductor (L_r) connected in series with a resonant capacitor (C_r), and this series branch is then connected in parallel with the magnetizing inductance (L_m) of the high-frequency transformer. The presence of the magnetizing inductance (L_m) gives rise to two characteristic resonant frequencies in the LLC converter.

The series resonant frequency of the LLC tank is determined by the resonant inductor and resonant capacitor as

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

The lower resonant frequency associated with the combined resonant and magnetizing inductances can be approximated as

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2}$$

Here, L_r is the series resonant inductance, C_r is the resonant capacitance, and L_m is the magnetizing inductance of the high-frequency transformer. The second expression is used as a simplified design-oriented approximation; the detailed dynamic behavior of the LLC converter still depends on the equivalent load and the selected operating point.

In general, the frequency f_m lies within the zero-current-switching (ZCS) region. Therefore, the system is designed to avoid direct operation in this region. Instead, the LLC converter exploits its resonant characteristics to achieve zero-voltage switching (ZVS) for the power semiconductor switches over the entire control range, thereby reducing switching losses and electromagnetic interference.

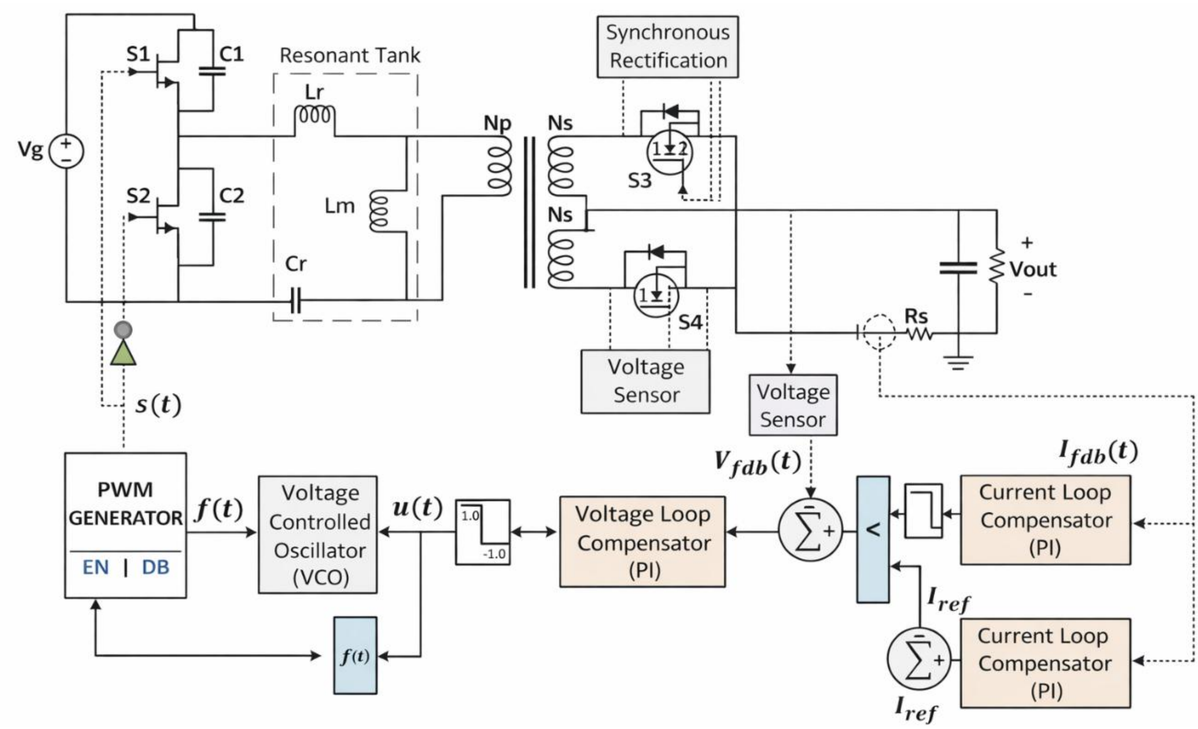


Figure 2. Circuit diagram of the half-bridge LLC resonant converter.

2.3. Signal Model Analysis

For the half-bridge LLC resonant converter, the development of a mathematical model requires more advanced analytical methods than those used for conventional PWM converters. In this study, the Extended Describing Function (EDF) method is employed to establish the small-signal model of the power stage around specified operating points [15].

Based on the obtained small-signal model, the open-loop transfer function of the system is derived and used as the foundation for the design of the feedback compensation network. On this basis, the parameters of the analog Type II compensator are calculated and tuned to ensure that the 60 VDC output voltage remains stable and returns to the regulated value without sustained oscillation when the load current undergoes abrupt variations.

3. Design of the Compensation Network for the LLC Resonant Converter

3.1. Theoretical Basis of the LLC Converters and Control Loop

The LLC resonant converter is a nonlinear system due to the presence of the resonant tank and the control mechanism based on varying the switching frequency. This nonlinear behavior makes the direct application of conventional linear control design methods difficult, particularly in the analysis of system stability and transient response. Therefore, to facilitate compensation design and control-loop analysis, the LLC converter must be linearized around a specified nominal operating point [16].

In this study, the small-signal model of the half-bridge LLC power stage is developed based on the EDF method. This method enables the effect of the switching-frequency control variable on the output voltage to be represented by an equivalent transfer function in the Laplace domain. As a result, the relationship between small perturbations in the control frequency and the resulting variations in output voltage can be described in a locally linear form, which is suitable for frequency-response analysis and feedback controller design.

The small-signal transfer function obtained from the EDF method captures the dominant dynamic characteristics of the resonant tank within the frequency range of interest, including the poles and zeros that govern the control-loop response around the selected operating point. Based on this model, the voltage control loop is designed to improve output-voltage regulation and transient response under the investigated load-change conditions.

3.2. Design Objectives of the Compensation Network

In power control systems, the design of a feedback compensation network generally pursues three fundamental objectives, including ensuring closed-loop stability, improving output-voltage regulation, and enhancing disturbance rejection capability. For the LLC resonant converter, the power stage inherently exhibits open-loop stability; therefore, the system can operate stably even in the absence of feedback control.

However, under open-loop operation, the ability of the LLC converter to monitor and regulate the output voltage is generally limited, particularly under rapid and large-amplitude load variations. Introducing a feedback loop improves output-voltage quality, but it also increases the system's sensitivity to control parameters, which may reduce the phase margin and potentially lead to instability if the compensation network is not properly designed.

Accordingly, the primary objective of the compensation design in this study is to enhance output-voltage regulation and disturbance rejection while preserving closed-loop stability within the investigated input-voltage and load-transient conditions [17, 18]

3.3. Selection of the Compensation Topology

In this study, an analog Type II compensator, consisting of two poles and one zero, is selected for output-voltage control of the LLC resonant converter. This compensation structure is widely used in power converters because of its ability to provide phase boost near the crossover frequency while maintaining a small steady-state error in voltage regulation.

Figure 3 illustrates the circuit configuration of the Type II compensator and its corresponding magnitude–phase characteristics on the Bode plot. The compensator includes one pole at the origin to provide high loop gain at low frequency, one zero positioned to compensate for the phase slope of the power stage, and one high-frequency pole to attenuate noise in the high-frequency range.

The transfer function of the Type II compensator is expressed as:

$$G_c(s) = K_c \frac{1+\dfrac{s}{\omega_z}}{s\left(1+\dfrac{s}{\omega_p}\right)} \tag{3}$$

where:

K_c is the gain of the compensator;

ω_z is the zero frequency, and;

ω_p is the high-frequency pole frequency.

The pole at the origin reduces the steady-state voltage error, the zero provides a phase boost near the crossover frequency, and the high-frequency pole limits the amplification of switching-related noise.

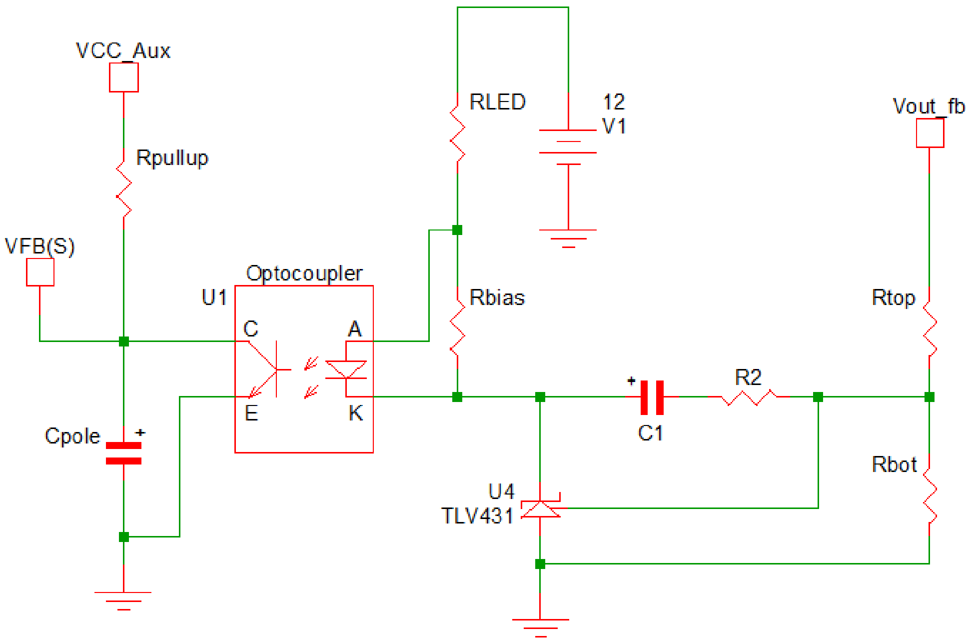


Figure 3. Circuit Diagram of the Feedback Loop With Two Poles and One Zero.

The actual compensation component values were selected according to the loop-gain target and then verified through SIMPLIS AC analysis. The detailed loop characteristics obtained from the compensated system are reported in Section 4.

The highest pole frequency of the compensator is selected according to the following expression:

$$\omega_p = K.\omega_c \tag{4}$$

where ω_c is the desired crossover frequency of the system, and K is the selection factor determined based on the phase characteristics of the power stage.

The crossover frequency of the compensator is determined as follows:

$$\omega_c = 2\pi f_c \tag{5}$$

The zero of the compensator is placed to offset the phase lag of the power stage at the crossover frequency and is determined by:

$$\omega_z = \frac{\omega_c}{K} \tag{6}$$

Based on the identified frequencies, the component values of the compensator can be calculated from the following relationships as:

$$R_c = \frac{K}{CTR.V_{err}} \tag{7}$$

$$C_c = \frac{1}{R_c.\omega_z} \tag{8}$$

where *CTR* is the current transfer ratio of the error amplifier block, and V_{err} is the output error voltage of the comparator circuit.

3.4. Simulation and Determination of Compensation Network Parameters

To evaluate the validity of the designed compensation network, a simulation model of a 500 W half-bridge LLC converter is developed in SIMPLIS, with the technical specifications listed in Table 1. The simulation model incorporates the complete power stage, control circuit, and feedback compensation network in order to accurately reflect the dynamic behavior of the system under practical operating conditions.

The parameters listed in Table 1 indicate that the half-bridge LLC converter operates over an input-voltage range of 370 - 410 VDC and delivers a regulated 60 VDC output. The rated output power is 500 W, corresponding to a rated output current of approximately 8.33 A. In addition, a 0 - 9 A short-duration load-step condition is considered to evaluate the transient capability of the compensation network under large-amplitude load disturbances. The system operates at a nominal switching frequency of 120 kHz.

Table 1. System parameters

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	370–410	VDC
Rated output voltage	V_o	60	VDC
Rated output power	P_o	500	W
Rated output current	I_o	8.33	A
Load-step test current	I_{step}	0–9	A
Nominal switching frequency	f_s	120	kHz

Detailed results on the frequency response and load transient response will be presented and discussed in Section 4.

4. Results and Discussion

4.1. Simulation Conditions and Parameter Setup

To accurately evaluate the closed-loop stability and transient response of the LLC converter, a simulation model was developed, as illustrated in Figure 4. SIMPLIS was used as a dedicated simulation tool for power converters because of its capability to analyze switching behavior and feedback-control components. The main technical parameters of the system were configured consistently with the experimental model, as detailed in Table 2.

In particular, to verify the operating capability of the Type II compensator under large-amplitude transient conditions, the load was configured as a step variation with an abrupt change from 0 A to 9 A. This condition represents a short-duration stress case rather than a continuous rated-power operating point. It emulates the startup or instantaneous load-disconnection condition of a BLDC motor, thereby enabling direct observation of the output-voltage undershoot, overshoot, and settling behavior.

Table 2. Design Parameters and Component Values of the LLC Converter

Parameter	Symbol	Value	Unit
Resonant capacitor	C_r	24	nF
Resonant inductor	L_r	100	μH
Magnetizing inductance	L_m	415	μH
Transformer turns ratio	$N_p: N_s$	3:1:1	—
Converter topology	—	Half-bridge LLC	—

4.2. Simulation Procedure

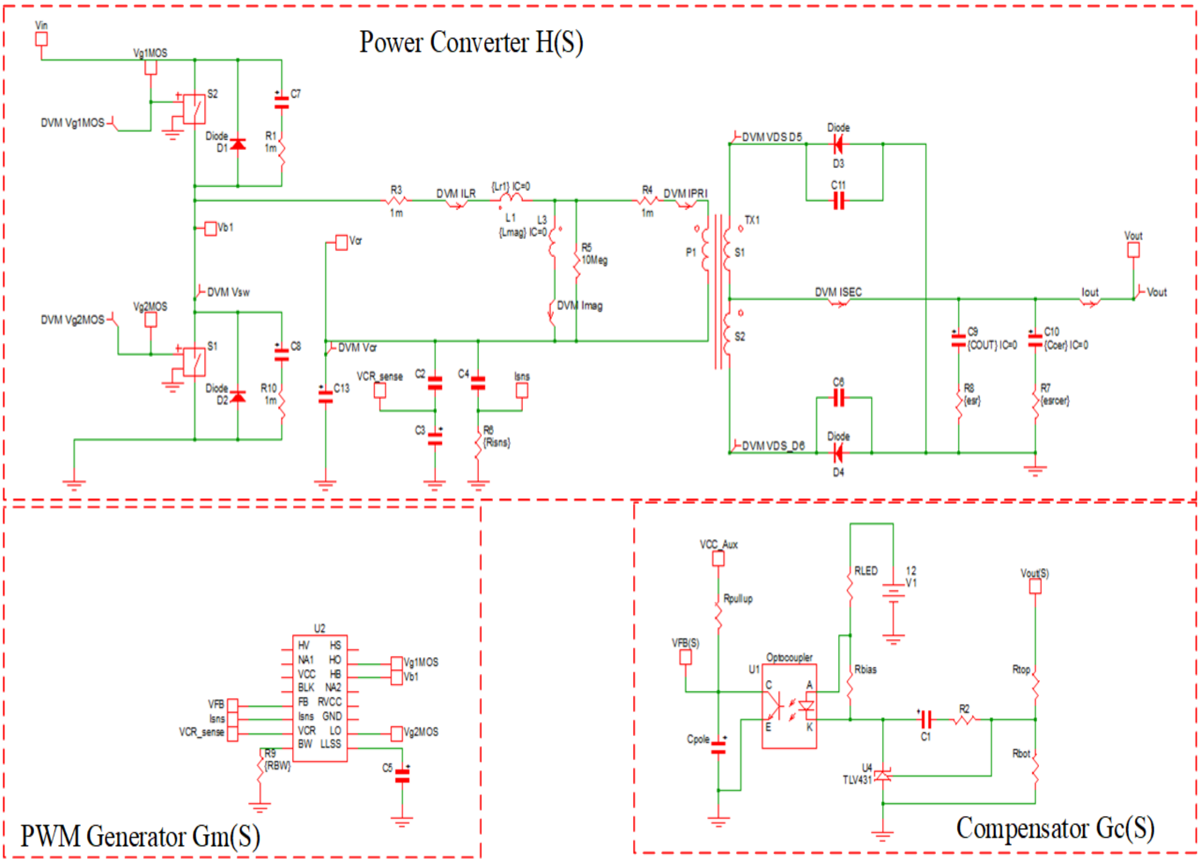


Figure 1. SIMPLIS Model of the 500 W Half-Bridge LLC Converter.

The simulation procedure was carried out systematically in SIMPLIS to verify the design parameters and the closed-loop characteristics. Figure 4 shows the SIMPLIS model of the 500 W half-bridge LLC converter.

The main steps are summarized as follows:

Power-stage modeling: The LLC half-bridge power circuit is modeled using two power switches, S1 and S2, driven alternately to generate a square-wave voltage applied to the resonant tank. The resonant network consists of the resonant capacitor C_r, implemented by capacitor C13; the resonant inductor L_r, corresponding to inductor L1; and the magnetizing inductance L_m of the transformer, represented by inductor L3.

Transformer TX1 provides galvanic isolation and voltage conversion. On the secondary side, a center-tapped transformer configuration is employed in conjunction with two rectifier diodes, D3 and D4. Output capacitors C9 and C10 are used to smooth and stabilize the output voltage. This step ensures that the simulation model accurately captures the nonlinear characteristics of the converter before subsequent analyses are performed.

Construction of the compensation network and feedback loop: To ensure system stability and fast dynamic response, a Type II compensation network was implemented on the secondary side. The compensator employs a TLV431 error-reference IC combined with an RC network (R2 and C1) to generate one pole and one pair of zeros.

Small-signal analysis and linearization: Periodic Operating Point (POP) analysis was performed in combination with AC Analysis to linearize the system around the nominal operating point (V_{in} = 390 VDC, P_{out} = 500 W). The resulting power-stage transfer function, H(s), serves as the basis for determining the gain and phase at the crossover frequency. Based on the frequency-response characteristics of the power stage, the Type II compensator was designed using the K-factor method. The R and C parameters of the compensator network were calculated to achieve a target crossover frequency, f_c, in the range of 3.89–4.6 kHz and an optimized phase margin, thereby ensuring stable operation without oscillation.

Frequency-response verification (loop analysis): A Bode plot of the overall open-loop transfer function (loop gain) was generated. This step was carried out to verify the actual crossover frequency and phase margin of the compensated system, ensuring compliance with gain-margin and phase-margin stability criteria.

Transient-response verification (time-domain analysis): Time-domain simulation was conducted under a load-step condition in which the load current abruptly changed from 0 A to 9 A (and vice versa). Key parameters, including voltage undershoot, overshoot, and settling time, were recorded to evaluate the quality of the output voltage supplied to the BLDC motor.

4.3. Analysis of the System Frequency Response

The frequency-response characteristics of the system were evaluated through SIMPLIS simulations at two input-voltage levels, 380 VDC and 410 VDC, corresponding to the minimum and maximum output voltages of the power factor correction (PFC) stage, respectively. Figure 5 presents the Bode plots of the voltage-control loop for the LLC resonant converter under these two operating conditions. The magnitude curve in the low-frequency region in Figure 5 exhibits high low-frequency gain, which helps reduce the steady-state error of the output voltage and maintain regulation around 60 VDC under the investigated load conditions. At the same time, the rapid gain roll-off in the high-frequency region enhances the system's immunity to sawtooth noise originating from the PWM modulation stage.

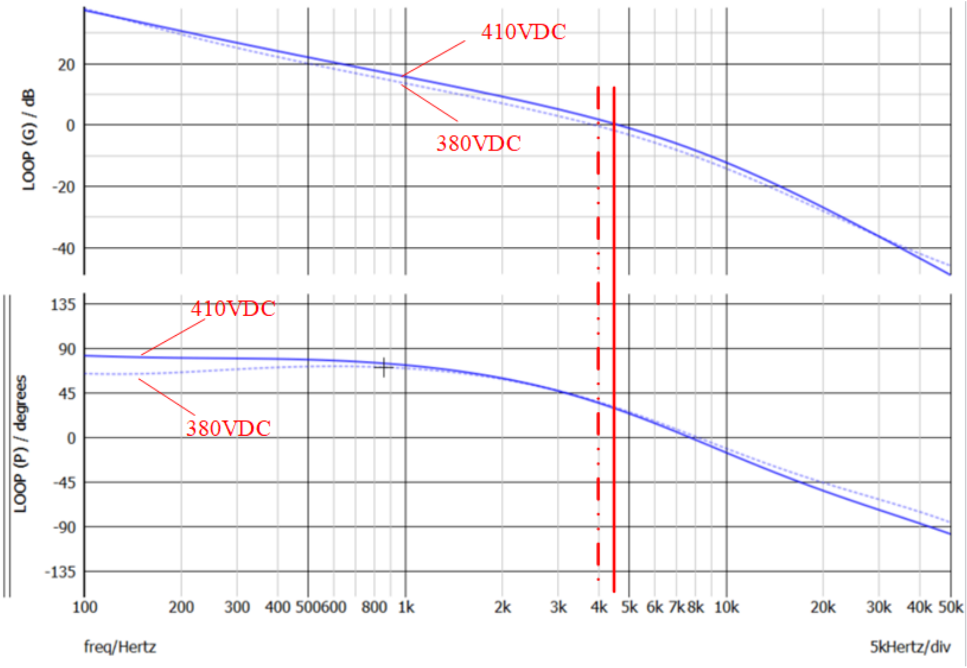
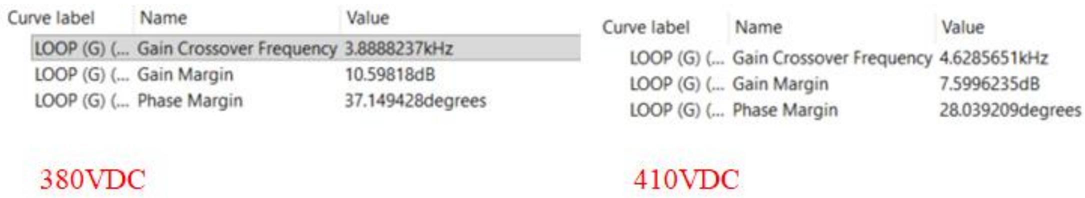


Figure 5. Bode Plot of the Compensated LLC Converter at Input Voltages of 380 VDC and 410 VDC.

The phase margin and gain margin values of the system are presented in Figure 6. At an input voltage of 380 VDC, the system achieves a crossover frequency of approximately 3.89 kHz with a phase margin of about 37°. When the input voltage increases to 410 VDC, the crossover frequency shifts upward to approximately 4.6 kHz, while the phase margin decreases to 28.3°. This variation reflects the influence of the operating point on the dynamic characteristics of the LLC power stage.



Curve label	Name	Value
LOOP (G) (...	Gain Crossover Frequency	3.8888237kHz
LOOP (G) (...	Gain Margin	10.59818dB
LOOP (G) (...	Phase Margin	37.149428degrees

380VDC

Curve label	Name	Value
LOOP (G) (...	Gain Crossover Frequency	4.6285651kHz
LOOP (G) (...	Gain Margin	7.5996235dB
LOOP (G) (...	Phase Margin	28.039209degrees

410VDC

Figure 6. Phase Margin and Gain Margin of the System at Different Input-Voltage Levels.

The minimum phase margin of 28.3° indicates a moderate rather than a large stability reserve. Therefore, the compensated loop should not be extrapolated beyond the tested operating range without further validation. Within the tested input voltage and load-step range, however, the measured and simulated responses do not show sustained oscillation. This observation is also consistent with the measured transient waveforms, where the output voltage returns to the nominal value without sustained oscillation.

To clarify the contribution of the proposed design, Table 3 compares this work with representative LLC-converter studies in terms of power level, load-transient condition, quantified control-loop design, switching-noise treatment, and intended application. This comparison is included to distinguish the proposed compensation design from previous studies that primarily emphasize steady-state analysis or limited transient validation.

Table 3. Comparison of the proposed LLC converter with related studies

Ref.	Converter configuration	Transient-control evidence	Noise treatment and application
[12]	Simulation-only full-bridge LLC resonant converter using SiC MOSFETs and a nonlinear adaptive sliding controller for a BLDC-drive system. No hardware prototype or clearly defined rated power was reported.	Voltage regulation, current response, BLDC speed and torque, step response, and harmonic performance were evaluated in MATLAB/Simulink. No experimental load-step validation or quantified loop crossover frequency and phase margin were reported.	The study addressed voltage regulation and system-level harmonic reduction for the BLDC drive. High-frequency switching-node ringing, parasitic-network characterization, and quantitative RC-snubber design were not experimentally investigated.
[13]	Experimental two-stage 1 kW PFC–LLC system with a nominal 400 V intermediate DC link and an output-diode-current-based mixed-signal control architecture.	A small-signal model and Bode-loop analysis were presented, together with experimental validation of input-voltage-disturbance rejection. A 360–400 V reference-step response was also reported. However, no 60 V, 0–9 A experimental load-step test was performed.	The main focus was twice-line-frequency input-disturbance rejection and reduction of the intermediate DC-link energy-storage requirement. Although the analog integration stages provided measurement-noise filtering, switching-node ringing, parasitic-network identification, and RC-snubber optimization were not investigated.
[14]	Experimental LLC resonant converter using automatic resonant-frequency tracking based on combined large- and small-signal models and an extended-state observer. The prototype operated at approximately 20 V input, 20 V output, and a 20 Ω load, corresponding to about 20 W.	Experimental parameter-step tests were conducted by changing the resonant capacitance, thereby shifting the resonant frequency between approximately 105 and 91 kHz. The proposed method demonstrated faster resonant-frequency tracking and lower output-voltage deviation than the compared methods. No experimental load-step test or quantified loop crossover frequency and phase margin were reported.	The study focused on resonant-frequency tracking under resonant-component variation. PCB parasitic inductance and resistance were mentioned qualitatively, but switching-node ringing was not quantitatively characterized and no RC-snubber design procedure was provided.
Our study	Half-bridge LLC converter, 500 W; 370–410 VDC input; regulated 60 VDC output.	0–9 A short-duration load-step test; K-factor-based Type-II compensator; f_c = 3.89–4.60 kHz; PM = 28.3°–37°.	Parasitic-induced ringing and RC-snubber effects are discussed as practical implementation issues. The targeted application context includes regulated BLDC-drive supplies and WPT downstream-regulation stages.

As summarized in Table 3, the related studies address different aspects of LLC-converter modelling and control. Reference [12] focuses on a simulation-based SiC LLC converter with nonlinear adaptive sliding control for a BLDC-drive system. Reference [13] presents an output-diode-current-based control architecture for improving input-voltage disturbance rejection in a 1 kW PFC–LLC system. Reference

[14] develops an automatic resonant-frequency-tracking method based on combined large- and small-signal models. These studies provide useful foundations for LLC-converter control; however, they do not report experimental validation under the same regulated 60 V, 500 W, 0–9 A short-duration load-step condition investigated in this work. Therefore, the comparison is intended to clarify the differences in design objectives and validation conditions rather than to imply a direct one-to-one performance ranking.

The comparison also highlights a practical aspect that is often not the main focus in conventional LLC-converter studies: the influence of switching-induced high-frequency disturbances caused by parasitic elements in the half-bridge power stage. Although the LLC resonant tank produces a quasi-sinusoidal resonant current, the MOSFET switching node still contains fast voltage and current transitions. These transitions may excite parasitic inductances and capacitances, resulting in drain-source voltage overshoot, high-frequency ringing, and narrow-pulse noise components with a wide frequency spectrum.

To mitigate these detrimental high-frequency effects and safeguard the switching devices from voltage overstress, effective transient suppression techniques must be employed. Consequently, an RC snubber network is integrated into the circuit topology to address these challenges. The primary parasitic components contributing to this phenomenon include:

Current Slew Rate (*di/dt*) and Parasitic Inductance (L_s):

Physical circuit components deviate from ideal characteristics due to parasitic elements, such as MOSFET package inductance, PCB trace inductance, and the leakage inductance of the resonant inductor. When a MOSFET turns off, the abrupt change in current (di/dt) interacts with these parasitic inductances, inducing a voltage overshoot characterized by the equation:

$$V = L_s \frac{di}{dt} \tag{9}$$

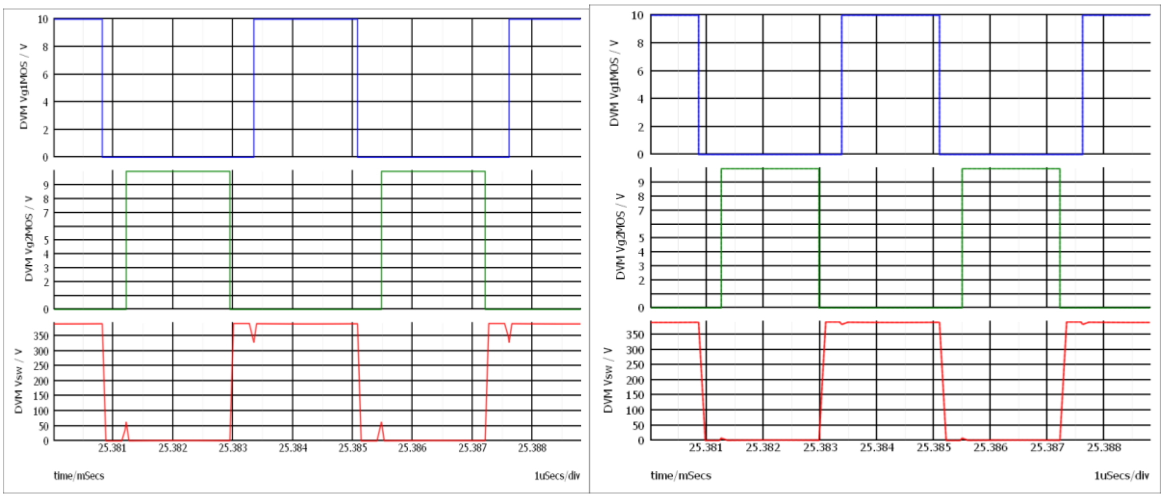
Parasitic Capacitance (C_{oss}): The parasitic capacitance (C_{oss}) of the MOSFET resonates with the parasitic inductances, establishing an unintended LC resonant circuit. This interaction generates high-frequency ringing that increases the Drain-Source voltage (V_{DS}) of the MOSFET. If the peak amplitude of this noise exceeds the breakdown voltage rating, catastrophic failure of the MOSFET can occur. Furthermore, this high-frequency noise can induce a voltage drop across the Gate resistor via the Gate-to-Drain capacitance, potentially triggering a false turn-on condition.

To mitigate the adverse effects of these parasitic components and suppress high-frequency noise, RC snubber networks (C7 and R1, C10 and R8 as illustrated in Figure 4) are implemented. The primary function of these networks is to absorb the energy from voltage transients and shift the resonant frequency, thereby dampening the peak Drain-Source voltage amplitude of the MOSFETs. Capacitors C7 and C10 function to reduce the voltage slew rate (*dv/dt*) across the MOSFETs. Resistors R1 and R8 provide critical damping by dissipating the resonant energy as heat, effectively preventing sustained oscillations between the parasitic inductance L_s and C_{oss}.

Figure 7a and Figure 7b present the waveforms simulated using SIMPLIS before and after the application of the snubber circuits, respectively. In these waveforms, DVM Vg2MOS represents the gate voltage of S1, DVM Vg1MOS denotes the gate voltage of S2, and DVM Vsw indicates the VDS of S1.

As shown in Figure 7a (without Snubber): Without the snubber network, significant voltage overshoots and severe high-frequency ringing are observed on the VDS waveform during the switching transitions. Figure 7b (with Snubber): Following the integration of the RC snubber circuits, the high-frequency switching noise is effectively suppressed, and the V_{DS} overshoot is virtually eliminated, ensuring stable and reliable operation.

Therefore, in addition to the K-factor-based Type II compensation design, this work discusses parasitic-induced switching disturbances as practical implementation issues, including the possible use of RC snubber-based damping where required. This discussion is important for applications involving rapid load variations, such as BLDC motor-drive supplies and downstream regulation stages in wireless power transfer systems, where the output voltage must recover without sustained oscillation.

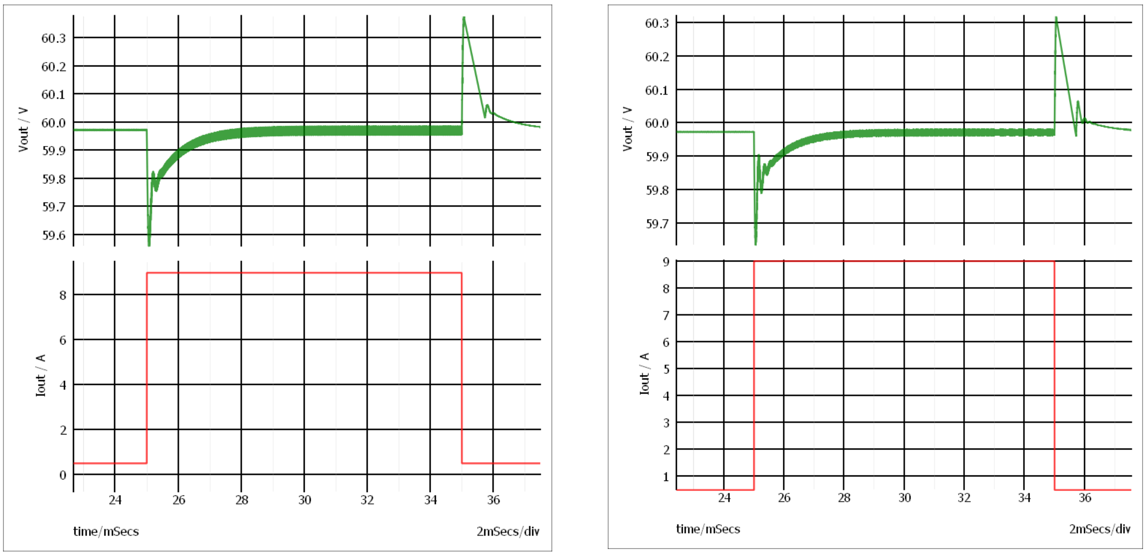


(a) (b)

Figure 7. Drain to Source Waveforms of S1: (a) Without Snubber and (b) With Snubber Circuit

4.4. Load-Transient response

The transient response of the system is evaluated under abrupt load-change scenarios, from no-load to full-load (0 A → 9 A) and from full-load to no-load (9 A → 0 A). Figures 8(a) and 8(b) present the simulated output-voltage responses corresponding to input voltages of 380 VDC and 410 VDC, respectively.



(a) (b)

Figure 8. Load-transient Waveforms at Input Voltages: (a) 380 VDC and (b) 410 VDC

In both cases, when the load current increases abruptly from 0 A to 9 A, the output voltage exhibits an undershoot. However, the undershoot amplitude remains limited, and the output voltage returns to its steady-state value. Similarly, when the load current decreases from 9 A to 0 A, the output voltage exhibits an overshoot, which is suppressed by the action of the control loop.

The simulation results show that, for both input-voltage levels, the output-voltage variation under the simulated load-transient condition is approximately ΔV_o = 370 mV, corresponding to less than 1% of the nominal 60 VDC output. This simulated value is used to evaluate the control-loop design before prototype testing; the experimental undershoot and overshoot values are reported separately in Section 4.5.

4.5. Experimental Results and Hardware Performance Evaluation

Based on the simulation results, a 500 W LLC resonant converter prototype was fabricated and tested. The experimental setup includes all major functional blocks, such as the PFC stage, resonant tank, control circuit, and dummy load, to reproduce practical operating conditions.

It should be noted that although the rated output power of the converter is 500 W, the 0–9 A load-step condition, corresponding to a peak output level of approximately 540 W at 60 V, was intentionally used as a short-duration stress test. This condition was selected to evaluate the transient response of the Type II compensation network under a large-amplitude load disturbance that may occur during BLDC motor startup or rapid load-mode transitions in WPT downstream regulation stages.

Figure 9 shows the fabricated half-bridge LLC converter prototype used for the experimental validation. Figures 10 and 11 present the measured output-voltage waveforms during load connection and load disconnection, respectively. When the load increases abruptly from 0 A to 9 A, the output voltage exhibits a maximum undershoot of approximately 938 mV. Conversely, when the load decreases from 9 A to 0 A, the output voltage shows an overshoot with an amplitude of approximately 705.5 mV. After each transient event, the output voltage rapidly returns to steady state without prolonged oscillation.

A comparison between the simulation and experimental results reveals consistent response trends, thereby supporting the validity of the design model and the role of the proposed Type II compensation network. Differences in the exact transient amplitudes are expected because the prototype includes non-ideal parasitic elements, measurement bandwidth limitations, and layout-dependent switching effects that are not fully captured by the simplified control-oriented model.

The simulation and experimental results indicate that the LLC resonant converter with the designed compensation network can maintain the regulated output voltage under the investigated input voltage and load-step conditions. The measured undershoot of 938 mV and overshoot of 705.5 mV correspond to approximately 1.56% and 1.17% of the 60 V output voltage, respectively. These values remain below 2%, indicating that the compensator improves the dynamic response of the system while preserving closed-loop stability under the investigated load-transient conditions.

Table 4. Verified closed-loop and load-transient characteristics of the compensated LLC prototype

Quantity	**Symbol**	**Value**
Input-voltage range	V_{in}	370 - 410 VDC
Rated output voltage	V_o	60 VDC
Rated output power	P_o	500 W
Short-duration load-step condition	I_o	0 - 9 A
Crossover frequency	f_c	3.89 - 4.6 kHz
Phase margin	PM	28.3° - 37°
Maximum measured undershoot	ΔV_{under}	938 mV
Maximum measured overshoot	ΔV_{over}	705.5 mV

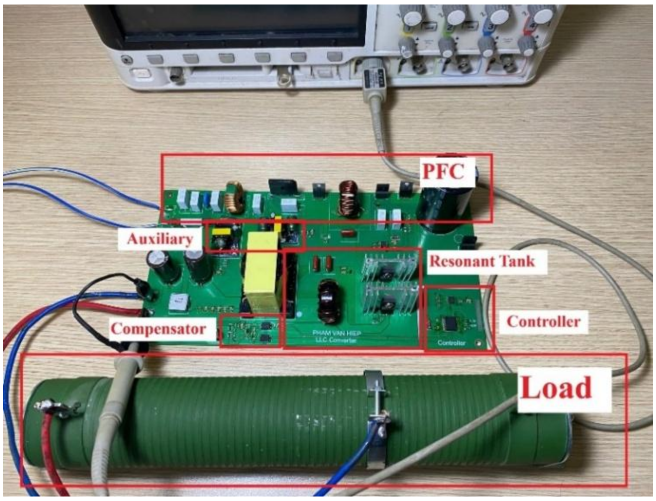


Figure 9. Fabricated 500 W half-bridge LLC converter prototype.

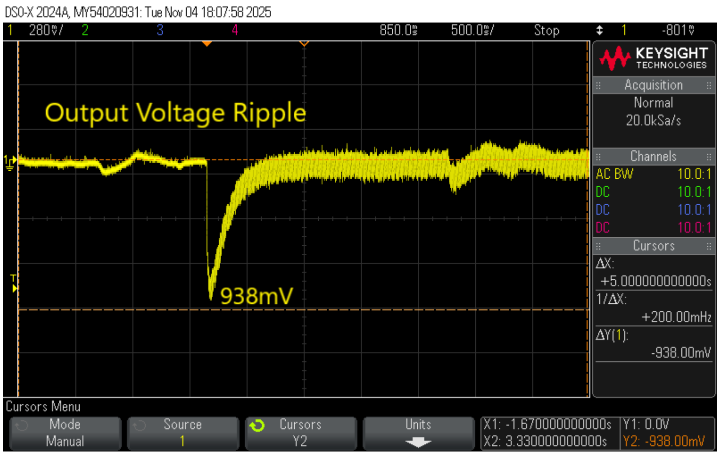


Figure 10. Measured output-voltage response during 0–9 A load connection.

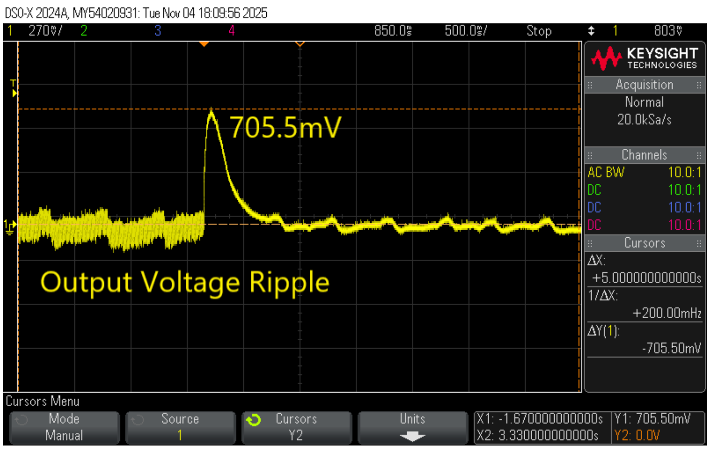


Figure 11. Measured output-voltage response during 9–0 A load disconnection.

These characteristics make the proposed converter particularly suitable for BLDC motor drive applications and wireless power transfer (WPT) systems, where the power supply is required to provide fast response and high stability during motor startup/shutdown or changes in operating mode.

5. Conclusion

This paper presented the design and experimental validation of a Type II compensation network for a 500 W half-bridge LLC resonant converter under rapid load variations. The compensator was designed using the K-factor method and verified through SIMPLIS-based frequency-domain analysis, time-domain load-transient simulation, and prototype testing. The converter maintained a regulated 60 VDC output within the investigated operating range under the 0 - 9 A short-duration load-step condition.

The measured undershoot and overshoot were 938 mV and 705.5 mV, respectively, corresponding to 1.56% and 1.17% of the nominal output voltage. The closed-loop crossover frequency was in the range of 3.89 - 4.6 kHz, while the phase margin varied from 28.3° to 37° over the tested input-voltage range. The minimum phase margin indicates a moderate stability reserve; nevertheless, no sustained oscillation was observed in the measured transient responses within the investigated operating range.

Future work should focus on increasing the phase margin, extending validation to wider load, input-voltage, and temperature conditions, and optimizing the layout and snubber design to further reduce switching-induced ringing. The use of next-generation semiconductor devices may also be considered to improve power density and efficiency.

References

[1] J. Zeng, G. Zhang, S. S. Yu, B. Zhang, Y. Zhang, LLC Resonant Converter Topologies And Industrial Applications- A Review, Chin. J. Electr. Eng., Vol. 6, No. 3, 2020, pp. 73-84, https//doi.org/10.23919/CJEE.2020.000021.

[2] G. A. Mudiyanselage, N. Keshmiri, A. Emadi, A Review of DC–DC Resonant Converter Topologies and Control Techniques for Electric Vehicle Applications, IEEE Open J. Power Electron., Vol. 4, 2023, pp. 945-964, https//doi.org/10.1109/OJPEL.2023.3331180.

[3] J. Shahsevani, R. Beiranvand, Application-oriented Review of the LLC-based Resonant Converters, IEEE Access, Vol. 12, 2024, pp. 52687-52726, https//doi.org/10.1109/ACCESS.2024.3386430.

[4] Y. Wei, Q. Luo, Z. Wang, H. A. Mantooth, A Complete Step-by-step Optimal Design for LLC Resonant Converter, IEEE Trans. Power Electron., Vol. 36, No. 4, 2021, pp. 3674-3691, https//doi.org/10.1109/TPEL.2020.3015094.

[5] M. F. Menke, J. P. Duranti, L. Roggia, F. E. Bisogno, R. V. Tambara, A. R. Seidel, Analysis and Design of the LLC LED Driver Based on State-space Representation Direct Time-domain Solution, IEEE Trans. Power Electron., Vol. 35, No. 12, 2020, pp. 12686-12701, https//doi.org/10.1109/TPEL.2020.2995942.

[6] J. S. Yoo, Y. M. Gil, T. Y. Ahn, Steady-state Analysis and Optimal Design of an LLC Resonant Converter Considering Internal Loss Resistance, Energies, Vol. 15, No. 21, 2022,. Art. no. 8144, https//doi.org/10.3390/en15218144.

[7] M. Ivankovic, LLC Design Guide: 600 W Converter—Simplified Algorithm Based on FHA and Vector Method, Infineon Technologies AG, Neubiberg, Germany, Appl. Note AN_2110_PL52_2110_182323, ver. 1.0, Nov. 2021.

[8] K. K. Geddam, E. Devaraj, Real-time Hardware-in-the-loop Implementation of LLC Resonant Converter at Worst Operating Point Based on Time-domain Analysis, Energies, Vol. 15, No. 10, 2022, Art. no. 3634, https//doi.org/10.3390/en15103634.

[9] J. Rocha, S. Amin, S. Coelho, G. Rego, J. L. Afonso, V. Monteiro, Design and Implementation of a DC–DC Resonant LLC Converter for Electric Vehicle Fast Chargers, Energies, Vol. 18, No. 5, 2025, Art. no. 1099, https//doi.org/10.3390/en18051099.

[10] S. Li, B. Fahimi, State-space Modelling of LLC Resonant Half-Bridge DC–DC Converter, IET Power Electron., Vol. 13, No. 8, 2020, pp. 1583-1592, https//doi.org/10.1049/iet-pel.2019.1503.

[11] M. Sucameli, C. Adragna, LLC Resonant Converters as Isolated Power Factor Corrector Pre-Regulators-Analysis and Performance Evaluation, Energies, Vol. 16, No. 20, 2023, Art. no. 7114, https//doi.org/10.3390/en16207114.

[12] G. M. Suba, M. Kumaresan, Design of LLC Resonant Converter with Silicon Carbide MOSFET Switches and Nonlinear Adaptive Sliding Controller for Brushless DC Motor System, Electr. Eng. Electromech., No. 4, 2022, pp. 34-43, https//doi.org/10.20998/2074-272X.2022.4.05.

[13] A. Maheshwari, F. Karakaya, A. Banerjee, J. S. Donnal, Control Architecture for LLC Resonant Converters With High Input Disturbance Rejection Capability Using Output Diode Current, IEEE Trans. Power Electron., Vol. 40, No. 1, 2025, pp. 652-664, https//doi.org/10.1109/TPEL.2024.3475251.

[14] R. He, B. Xue, M. Zhou, M. Fu, J. Liang, Y. Liu, H. Wang, Resonant Frequency Tracking Scheme for LLC Converter Based on Large- and Small-signal Combined Model, IEEE Access, Vol. 11, 2023, pp. 83390-83399, https//doi.org/10.1109/ACCESS.2023.3301850.

[15] A. Lordoglu, M. O. Gulbahce, D. A. Kocabas, S. Dusmez, Extended Describing Function Modeling and Closed-Loop Control of LLC Converter in Battery Charging Applications, in Proc. 2021 Int. Aegean Conf. Electr. Mach. Power Electron. (ACEMP) and Int. Conf. Optim. Electr. Electron. Equip. (OPTIM), Brasov, Romania, 2021, pp. 274-279, https//doi.org/10.1109/OPTIM-ACEMP50812.2021.9590032.

[16] Y. Zhang, X. Ruan, Discrete-time Small-signal Modeling of LLC Resonant Converter Considering the Nonlinearity of Voltage-controlled Oscillator, IEEE Trans. Ind. Electron., Vol. 71, No. 4, 2024, pp. 2416-2428, https//doi.org/10.1109/TIE.2023.3269469.

[17] A. Nabih, M. H. Ahmed, Q. Li, F. C. Lee, Transient Control and Soft Start-up for 1-Mhz LLC Converter with Wide Input Voltage Range Using Simplified Optimal Trajectory Control, IEEE J. Emerg. Sel. Topics Power Electron., Vol. 9, No. 1, 2021, pp. 24-37, https//doi.org/10.1109/JESTPE.2020.2973660.

[18] X. F. Wei, B. Zeng, M. Jiang, C. G. Huang, Dynamic Behaviors and Stability Analysis of Closed-Loop Controlled LLC Resonant Converters, Electronics, Vol. 15, No. 3, Art. no. 706, 2026, https//doi.org/10.3390/electronics15030706.