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Novel Low-Complexity CCK Decoder for IEEE 802.11b System

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Abstract. A novel low-complexity decoder for Complementary Code Keying (CCK) modulation is proposed in this study. Compared to the decoder architecture based on Fast Walsh Transform (FWT), the presented architecture requires less resource on hardware and still keeps reasonable performance of system. By mapping complex chips to modulo-4 numbers and decomposing coded words by in-dependent angle parameters based on theirs different properties, the proposed method allows a faster and more direct decoding for those parameters than traditional method.

Keywords: CCK, FWT, IEEE 802.11b

1. Introduction

The IEEE 802 11b [1] is a standard for wireless local area network (WLAN). It has four kinds of data rate: 1-2 Mbps by using Baker sequence and 5.5-11 Mbps by using Complementary Code Keying (CCK) modulation. CCK is a variation on M-ary Orthogonal Keying modulation which uses an I/Q modulation architecture with complex symbol structures. CCK allows for multi-channel operation in the 2.4 GHz ISM band by virtue of using the existing 802.11 1-2 Mbps direct sequence spread spectrum (DSSS) channelization scheme. The spreading employs the same chipping rate and spectrum shape as the 802.11 Barker words spreading functions, allowing for three non-interfering channels in the 2.4 to 2.483 GHz band.

The CCK modulation included 64~256 code word of 8-complex chips [2]. Those words are closely orthogonal to each other and have identical properties as those of the Walsh code. Each code word corresponds to one of the combinations of 8 data bit. At the receiver side, the received complex symbols are decoded in order to recover the original information.

Fast Walsh Transform (FWT) [1, 2] is used to decode the complex symbols. The architecture based on FWT can reduce a certain number of complex adders when compared to the direct architecture based on 256 sets of correlations. However, this design has to find the maximal output from total 256 correlation values. Generally, the area for a 256 input comparators is large formatter will need to create these components, incorporating the applicable criteria that follow.

The "pipelined CCK decoder" [3] was designed to reduce the complexity of CCK decoder based on FWT. The idea based on the fact that the CCK chips are sequentially received and on carefully accounting the data flow and scheduling of the correlation

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operations in the decoding process. The new method has fewer adders than those of FWT-based architecture and needs only a small number of comparators and small associated area. It also has simple control and high efficiency.

The fact that all of the code words carry the in-dependent parameters φ_i (i=1,2..,4) equal the different values of chips is utilized. In addition, the CCK code has redundant property for communications. That is, the independent parameters are repeated four times in one of the code words. The proposed method does not search all possible values of in-dependent parameters and then choose the value giving the best matching between received symbol and available code word. Instead, based on different values of chips, this method directly decides the in-dependent parameters and emphases them by their repeated numbers. The method therefore has lower complexity and runs faster.

This paper is organized as follows. Section II introduces about the CCK modulation and demodulation scheme. Section III proposes the novel low-complexity CCK decoder and explain it's operation. In section IV the comparisons between past architectures and the proposed design are made. Finally, a summary is given in section V.

2. CCK modulation and demodulation in 802.11b

Here we assume that CCK code of 11Mbps is used. Its details are provided as follows:

A. CCK modulation

Each CCK symbol includes 8 bits (b_0~b_7). The first dibit (b_0b_1) encodes φ_1 based on DQPSK modulation, as specified in Table 1, and the remaining dibits (b_2b_3),(b_4b_5),(b_6b_7) encode phases φ_2, φ_3, φ_4 based on QPSK modulation as specified in Table 2.

In the CCK modulation, There are 8 complex chips (c_0~c_7) in each code word symbol c (includes 8 data bits). They are made based on the following formula [4]:

$$c = (c_0, c_1, c_2, c_3, c_4, c_5, c_6, c_7,)$$
$$= \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, -e^{j(\varphi_1+\varphi_4)},$$
$$e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j(\varphi_1)}\} \quad (*)$$

Here φ_i (i=1~4) is the in-dependent parameter and can get 4 values $\{0,\pi/2,\pi,3\pi/2\}$ as stated in table 1,2.

Table1. DQPSK encoding table for the first dibit

Dibit(d_0d_1) (d_0 is first in time)	**Phase change**	
	Even symbols	***Odd symbols***
00	0	π
01	π/2	3π/2
10	π	0
11	3π/2	π/2

Table 2. QPSK encoding table

Dibit pattern[d_id_{i+1}]	**Phase**
00	0
01	π/2
10	π
11	3π/2

Notes that by that way, every chip in a code word can receive 4 values {1,-1, j,-j}, so there is a total of 4^8=65536 different combinations of 8 chips. The CCK codes are 256 code words which have chosen from above combinations based on four in-dependent parameters φ_1, φ_2, φ_3, φ_4 (4^4=256) and equation (*). By this way, code words keep their orthogonal property like those in Walsh Code. Those 256 code word can be encoded for 8 bits of data.

As such, CCK code is similar to the M-rank code in communications and does not need any additional bandwidth, but it can provide a data rate log2M times higher than that of Barker spread code. Besides, they can well tolerate the multi-path effect in transmission.

From equation (*), one can observe that φ_1 is a common factor of all chips, φ_2 appears in all odd chips, φ_3 is add to all odd pairs of chips and φ_4 appears in the first four chips.

B. CCK demodulation based on FWT

The four phase variables each take on values of $\{0,\pi/2,\pi,3\pi/2\}$, and there are 256 (4*64) possible 8 chip codes. These codes have an inherent "Walsh" type structure that allows a simple butterfly implementation of the decoder. Although it is possible to squeeze a few more complementary codes out of this 8-chip set, the rest of the codes cannot be decoded with the modified fast Walsh transform.

When decoding a received CCK symbol, has to find the most matched one among the 256-candidate code word. But all chips have common factor φ_1, so only needs to search among 64 sets of code word to decode phases φ_2~ φ_4 first and then decode phase φ_1.

The conventional approach using FWT [5] is composed of four basic sub-blocks, which is shown in figure (1). The sub-block structure, which decodes φ_3, φ_4 for given φ_2, is shown in figure (2).

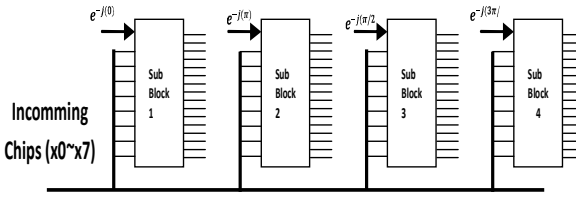

Fig. 1. CCK decoder architecture based on FWT.

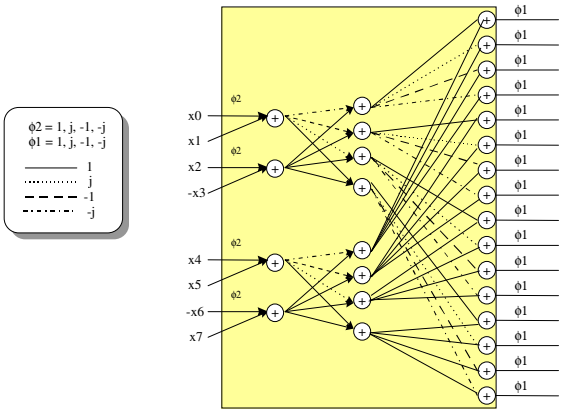

Fig. 2. The structure of basic subblock module.

This decoder can reduce adder areas in doing directly the correlation operation. Still, after FWT, phase φ_1 needs to be multiplied with the output of each FWT sub-block. As such, one needs to do a 256-operand comparison operation and find out the maximum one.

C. CCK demodulation based on pipeline

The model of "Pipelined CCK decoder" is presented in Fig. 3. [3]

This model is explained as follows. There are 8 basic pipelined sub-blocks, each calculates the correlation values of 32 sets of code word with the received samples, {x0~x7}. Since is common to all chips, it can be factored out temporarily and excluded in the calculation of the correlation values. Therefore, each sub-block deals with eight intermediate code word first and generates eight intermediate correlation results in a pipelined fashion.

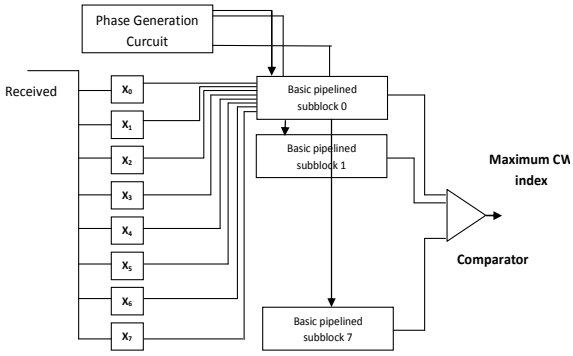

Fig. 3. The Pipelined CCK decoder model.

After that each intermediate correlation result is multiplied with four 4 different possible φ_1 values so four complete correlation results will be obtained and compared in the "selector" cell to get the maximum one. The "selector" determines the specific phase in four possible values $\varphi_1=\{0°, 90°,180°, 270°\}$ that maximizes the value of $\mathrm{Re}\{Corr_i \sim e^{-j\varphi_i}\}$, for each code word, where Re denotes the real part of variable *x*.

In summary, there will be eight local maximum values entering the final comparator cell in each sub-block. The comparator then performs the comparison operations on the eight serially coming-in local maximum values and find out the maximum value. As result, in the final stage of the entire CCK decoder there needs an eight-input comparator that selects the global maximum from the eight local maximum values produced by the eight basic pipelined sub-blocks. This maximum value and its associated index provide the decoded code word.

3. Proposed decoder for CCK demodulation

A. At transmitter side

At first, 4 values $\{0, \pi/2, \pi, 3\pi/2\}$ of every $\varphi_i(i=1\sim 4)$ are mapped to 4 values 0,1,2 and 3. Any additive operation of φ_i (i=1- 4) then corresponds to an additive operation of modulo-4 numbers. Moreover, any subtractive operation corresponds to an additive operation with the complement of 4.

For example:

$\pi+3\pi/2=5\pi/2$ equivalent to $\pi/2$, corresponds to 2+3=5 which is equivalent to 1 (modulo 4).

$\pi-3\pi/2= -\pi/2$ equivalent to $3\pi/2$ corresponds to 2-3= -1 which is equivalent to 2+ (1) =3 (modulo 4)

Secondly, the values of φ_i (i=1~4) are derived by Table 1, 2 based on the arrived data (b_0~b_7). Then they are calculated by equation (*) under the form of modulo-4 numbers to make 8 complex chips of one code word also under form of modulo-4 numbers.

Finally, by using the look-up table, the values {0,1,2,3} are mapped to the pairs (1,1), (-1,1),(-1,-1),(1,-1) then they are divided to branch I and Q in QPSK modulation for transmission.

B. At the receiver side

The samples of chip are sampled simultaneously at branch I and Q, then decided to the value pairs of (1,1),(-1,1),(-1,-1),(1,-1). After converting those pairs to the modulo-2 numbers (11), (01), (00), (10) they are mapped to values of {0, 1, 2, 3}. Those numbers correspond to values of complex chip (c_0~c_7) under the form of modulo-4 numbers.

The decoded method is presented in Fig. 4. After that, the following operations are calculated to give the results in the ideal case of transmission

$c_0-c_1= c_2-(-c_3)= c_4-c_5= (-c_6)-c_7= \varphi_2$ (modulo 4)

φ_2 is again converted to values of $\{0, \pi/2, \pi, 3\pi/2\}$ and then mapped to b_2b_3 as the table 2. That means we have decoded b_2b_3.

Note that the parameter φ_2 is repeated four times in each code word. Therefore, if there are errors caused by transmission then the decision of φ_2 is done by majority rule. That means, if one of the values calculated for φ_2 is not equal to the three remaining identical values of φ_2, then the decision of φ_2 is chosen based on those three. In the case when we have two values for φ_2 repeated two times, then the decision is done with the error probability of 50%

To implement decisions with majority rule, the modulo-4 numbers of φ_2 again are converted to modulo-2 numbers. The majority rule is implemented separately on the bits having the same position. For example, four numbers of modulo-2 are 01,10,10,10. So 4 first bits in the same position are 0,1,1,1 and 4 second bits are 1,0,0,0. By averaging those numbers and rounding to 1,0, the majority law is implemented and we have the number of 10.

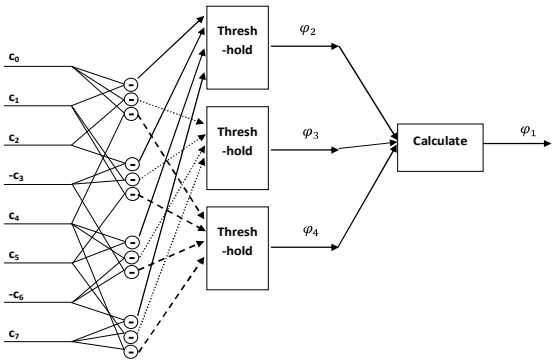

Fig. 4. The novel CCK decoded method.

Finally, after decisions made by majority law, φ_2 again is converted to{0,1,2,3}mapped to b_2b_3.

By analogy method the φ_3, φ_4 are calculated as follow:

$$c_0\text{-}c_2= c_1\text{-}(\text{-}c_3)= c_4\text{-}(\text{-}c_6)= c_5\text{-}c_7= \varphi_3 \text{ (modulo 4)}$$

$$c_0\text{-}(c_4)= c_1\text{-}c_5= \text{-}c_3\text{-}c_6= c_4\text{-}c_7= \varphi_4 \text{ (modulo 4)}$$

Finnaly, φ_1 is specified last, after receiving values of φ_2 ,φ_3 ,φ_4:

$$\text{-}c_3\text{-}\varphi_4=c_5\text{-}\varphi_3=\text{-}c_6\text{-}\ \varphi_2= c_7= \varphi_1 \text{ (modulo-4)}$$

From here all of CCK symbol are recovered.

4. Implementation and performance evalution

The design of the CCK modulator and demodulator using the proposed method is implemented on Xilinx's Tools for FPGA.

A. Implementation

Pairs of two bits from a random binary generator are concatenated for modulo-4 numbers. Those numbers are separated by a de-multiplexer with 4 outputs (b_0b_1, b_2b_3, b_4b_5, b_6b_7). Duration of output's number equals 8 time bit's clock. They are the values to make the phases φ_i (i=1~ 4). Under the clock's control, the phases are added to make 8 complex chips or a CCK code word as equation (*). A unit "Addr" is added to make sure that the additional operation is the modulo-4 adding. Two "Addr" follow are mapped to two branch I and Q. Design for the demodulator is showed in Fig. 3.

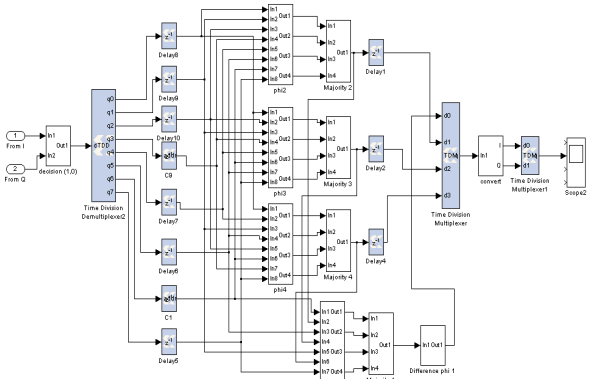

Fig. 5. Design for modulator using System Generator in Matlab.

The samples from branch I and Q are decided with a threshold zero. They are then concatenated to convert the dibits to modulo-4 numbers. A de-multiplexer separates serial chips to 8 parallel chips (c_0~c_7). The calculations between chips are carried out for recovering phase φ_i. After "majority" unit they are multiplexed then mapped to values of b_0b_1, b_2b_3, b_4b_5, b_6b_7.

The simulation is carried out on AWGN channel and compared with two cases: using majority law and not using it. The majority law is based on the majority results and the other method is based on the random results from the group of four results.

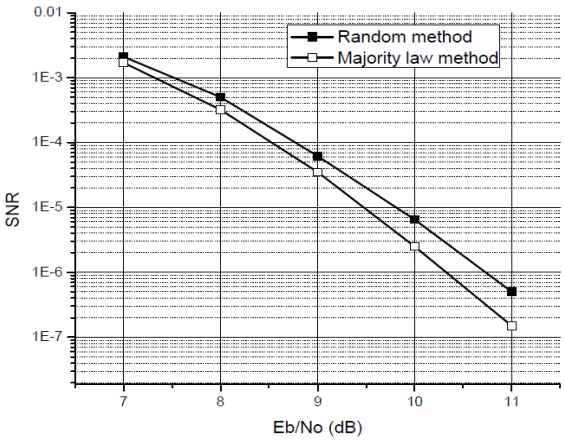

Fig. 6. Comparison the system performance between two case: using majority law and random method.

Of course that the performance of system based on majority law is better then case of random law. For comparision the performance of proposed method and existing CCK deceders, we chosed HFA3860B as the reference system. The BER of our proposed and HFA3860B CCK decoder is shown in Fig. 7

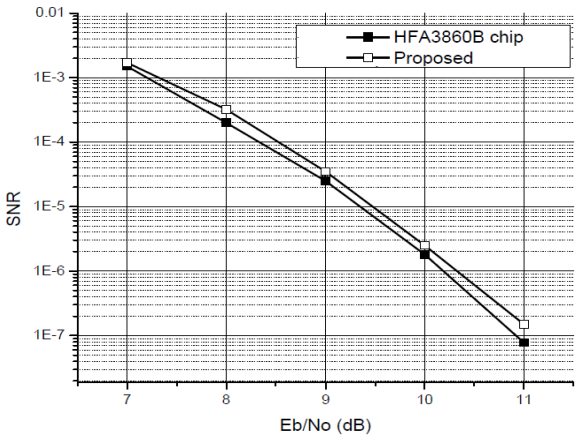

Fig. 7. Comparison between HFA 3860B chip and our proposed.

B. Comparison of the hardware resource

In our proposed method, the parameters phase φ_i are calculated and decided directly. No searching in all of the possible phase values is done. Therefore, there are only 8 real adders for calculation of one phase and 4 real adders for majority. In addition, there are 12 comparators, 6 shifters and 2 multiplexers. The total resource consumed is much less than that of the method FWT.

5. Conclusion

In this study, we propose a low-complexity CCK decoder. It exploits the following property of a code word: different value of chips carries the information of phases. Besides, the repeated property of the phase in one code word is used for a higher reliability. In comparison with the FWT method, the proposed method needs less hardware resource and still keeps reasonable performance in transmission.

Acknowledgments

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Bộ giải mã CCK mới với độ phức tạp thấp cho hệ thống IEEE 802.11b

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Bộ giải mã mới, độ phức tạp thấp cho điều chế Khóa mã bù (CCK) được đề nghị trong bài báo này. So sánh với những kiến trúc giải mã dựa trên biến đổi Walsh nhanh (FWT), kiến trúc được trình bày yêu cầu ít tài nguyên phần cứng hơn mà vẫn giữ được hiệu quả của hệ thống. Bằng cách ánh xạ các chíp phức vào số modulo-4 và phân ly từ mã theo các tham số góc độc lập dựa trên tính chất khác nhau của nó, phương pháp đề nghị cho phép giải mã nhanh hơn, trực tiếp hơn và độ phức tạp thấp hơn so với phương pháp truyền thống.

Từ khóa: CCK, FWT, IEEE 802.11b.